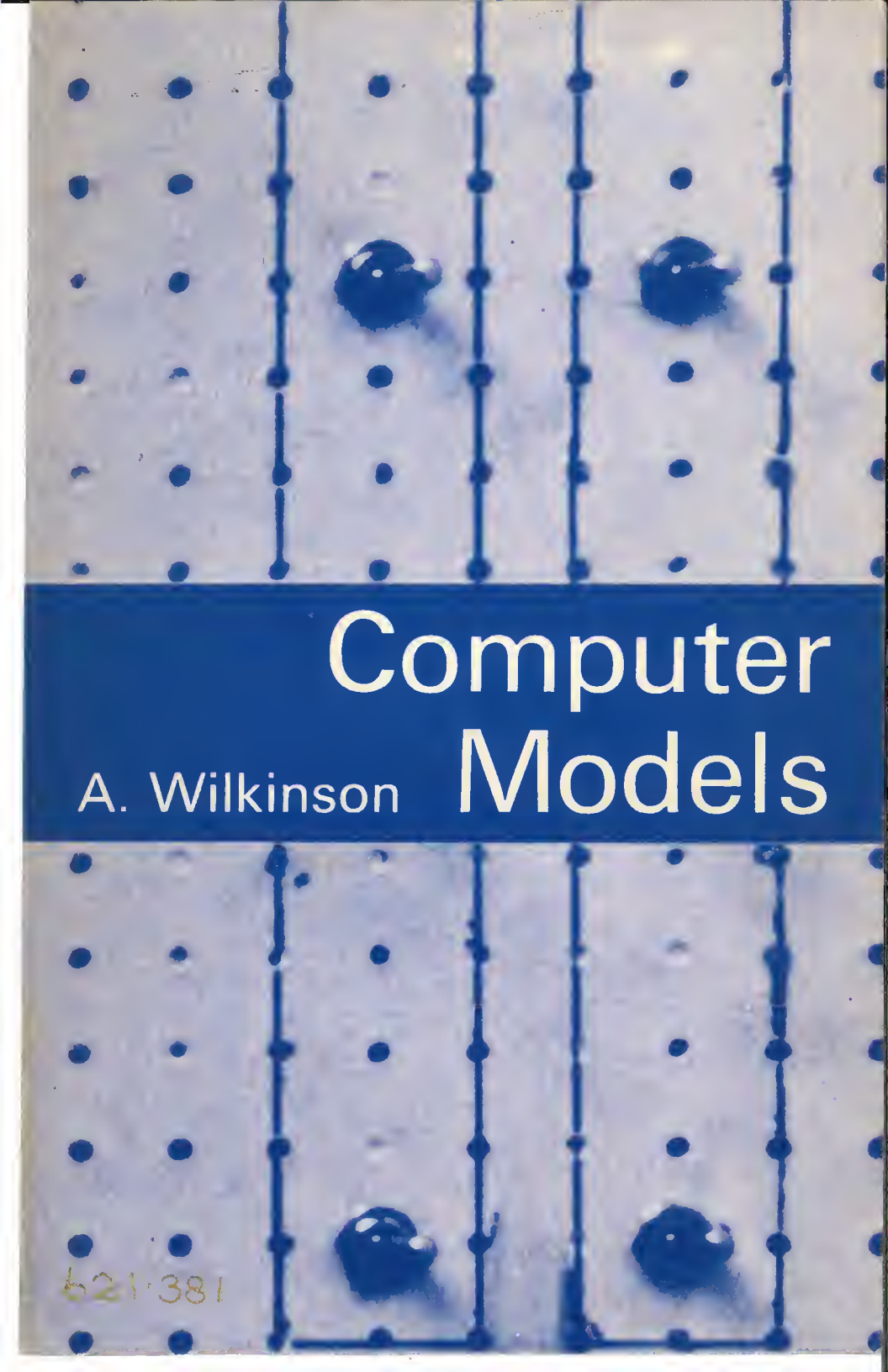

Computer Models

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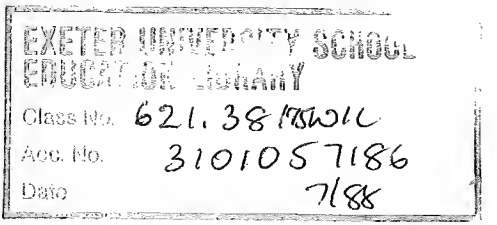
EDWARD ARNOLD (PUBLISHERS) LTD

First published 1968

SBN: 7131 1505 X



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Preface

The computer models described in this book have all been built, tested and operated by pupils of the Grammar Technical School, Spennymoor. The aim, initially, was to provide an enjoyable out-of-school activity which would also have a bearing on some of the modern applications of mathematics. However, far more than this has been achieved. Those taking part in the projects have not only experienced some of the thrills and frustrations of research work but also gained an insight into modern electronic circuits. In addition, those not taking an active part have had the opportunity to see and operate working models which give an insight into the high-speed world of electronics. All this helps to breed a confidence which cannot be achieved in any other way.

The models range from a cheap mechanical model through a logic demonstration board to a high-speed computer model. All the electronic models are based on the NOR logic element and no advanced knowledge of electronics is necessary to construct them and none at all to operate them.

Many of the units have been used to demonstrate principles of binary number work, statistical distributions and simple logic to students with no knowledge of electronics. It is felt that these models can be of particular use in schools where a modern mathematics syllabus is being followed and also in colleges running a general mathematics course. In addition, only a small amount of ingenuity should be needed to make use of these units in a variety of experiments where small time measurements are required.

A.W.

Acknowledgements

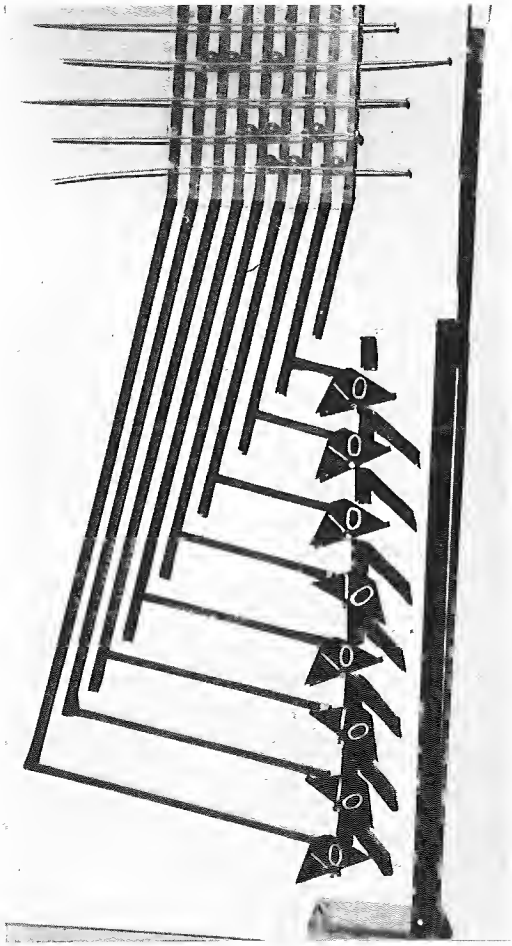
I should like to thank the following:
Dr. L. Molyneux and Mr. G. Flanagan of Newcastle University for permission to use their basic NOR logic circuit.
Mr. G. Flanagan for a considerable amount of help both with the manuscript and with the circuits described in the book.
Mr. D. Toon for many of the photographs.
Mr. K. Dart of Gosforth Grammar School and my colleague
Mr. J. C. Bainbridge for helping to read the manuscript.

Contents

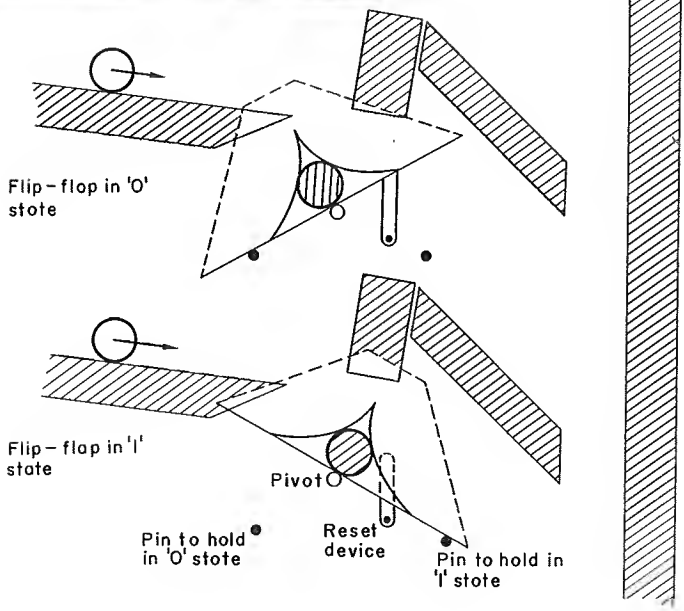
CHAPTER I

A Ball-Bearing Computer

The ball-bearing computer uses ball-bearings to represent electrical pulses. The photograph (page 8) shows the layout of the model which is mounted vertically and stands about three feet high. Near the top of the model the ball-bearings can be arranged in rows to represent binary numbers. Three such rows are shown, each resting on a knitting needle. When the needles are withdrawn the balls drop from the store down channels into the machine. The arrangement is similar to the store in a computer in that it holds a set of numbers to be fed into the arithmetic unit of a computer at an appropriate time. On the right hand side of the board is a series of mechanical flip-flop devices arranged in a vertical line. Each flip-flop rotates through approximately 60° about a central pivot and is at rest with either the left or right hand side uppermost. In one position the '0' digit is uppermost while in the other the '1' digit is uppermost. Each flip-flop can therefore register either '0' or '1'. Balls released from the 'store' fall down an almost vertical channel into one with a gradual slope. The momentum acquired during the fall is virtually destroyed and the ball rolls gently into the flip-flop device. On entering the flip-flop, the ball causes it to change its state. If the state was '0' then the device flops over to '1' and the ball leaves to the right and falls into the small container at the foot of the board. If, however, the ball enters one in the '1' state it causes it to flip to the '0' state whereupon the ball leaves the device on the left and falls to the channel below and rolls gently into the next flip-flop. The reader will realise that the uppermost flip-flop represents the least significant digit and the lowest flip-flop represents the most significant digit of a binary number represented by this vertical column of flip-flops. The action of the ball which falls from one flip-flop to a lower one represents a carry-over operation in addition. The diagram at the foot of page 8 gives more detail of these mechanical flip-flops and the associated channels.



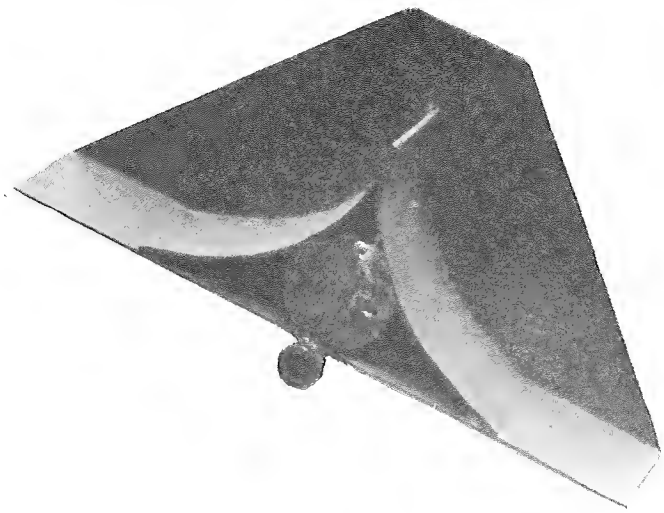
The Ball-Bearing Computer.
The model shown is arranged to add the three binary numbers 1101, 11010, 1101000 to the number in the vertical register, i.e. 1101000.
The three binary numbers at the top of the board show the arrangement necessary for multiplying 1101 by 1011, i.e. (1101 × 1) + (1101 × 10) + (1101 × 0) + (1101 × 1000). The model will give the product of 1101 and 1011 if the balls are released into an empty vertical register.



The whole model can be covered with a glass sheet which allows all operations to be observed and which also prevents balls from leaving the model prematurely. Since only the digit which is upright on the flip-flop is to be considered in any result, the other digit can be hidden from view by a small black painted area on this covering sheet.

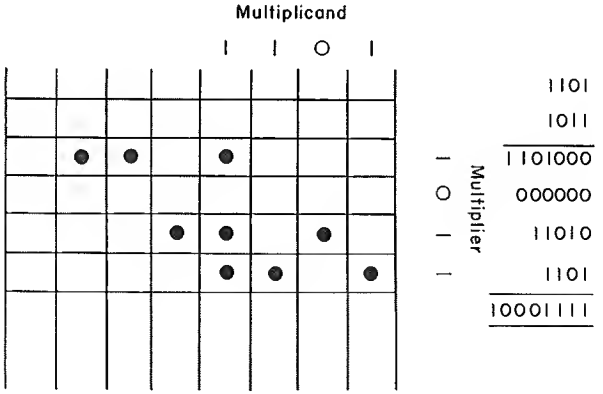
Addition, and the processes of multiplication, can be demonstrated on the board. A ball to represent '1' and no-ball to represent '0' are arranged in horizontal rows and held in position by knitting needles which are pushed through slots in the 'store'. These numbers are released into the arithmetic unit by withdrawing the needles from left to right. This operation should be carried out slowly so that balls working their way through the model should not be in collision and, in particular, two balls should never enter a flip-flop together and so be counted as one. The action just described is similar to that which takes place with electrical pulses in a real computer—the row of balls moving through the flip-flops is replaced by a pulse train which works at a speed of about one million times as fast as this model.

The numbers shown arranged in the photograph opposite are, reading from bottom to top, 1101, 11010, 11010000, or, in decimal 13, 26, 104 which can also be written as 13×1, 13×2, 13×8. This is simply the binary number followed by shifts of 1 and 3 to the left. As the operation of multiplication depends on this shifting process it is



Rear view of one mechanical flip-flop.

possible to demonstrate this operation. The diagram below should be familiar to anyone who has multiplied in any number system but it will be seen that, in the binary system, we are only concerned with multiplication by 1 or 0 and so the multiplicand appears over and over again at points where multiplication by 1 is involved while blank spaces appear when 0 is involved.



CHAPTER II

The NOR Logic Element

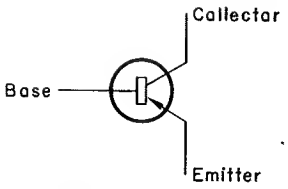
Earlier books in the *Contemporary School Mathematics Series* have shown how Boolean Algebra can be used to create mathematical models of switching circuits and, conversely, how these functions can be represented by these circuits. We can now show the high speed type of switch used in computer circuits and build up the Boolean functions to represent these circuits.

One switch used in modern computers is a solid state device, based on the transistor. The transistor has a number of very valuable properties which are not common to the normal mechanical device. It is small, involves no moving parts, is robust, reliable and capable of very high speed switching in the order of 1,000 times faster than the best mechanical switch. The operating voltage and the current flowing through the device are low and, once installed in a circuit, can be expected to have a very long life much in excess of any mechanical component.

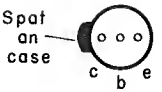
Our model computer will be built up from NOR logic elements, but before we define this element, and in order to understand more fully the working of the NOR logic element, it is necessary first to understand a little about the construction and working of the transistor. Although two main types of transistor are manufactured, one made from silicon, the other from germanium, in the following paragraphs we will be referring only to the former.

The transistor is a three terminal device in which the current flowing between two of the terminals can influence the current flowing between a further pair. The symbol used for this component is shown in the diagram at the top of page 12, together with a diagram of a typical silicon transistor, the Mullard OC200.

The three leads or terminals from the transistor are connected inside the device to a small piece of semi-conductor material, and are known as the emitter, base, and collector, respectively. Inside the transistor the semi-conductor material is slightly modified during



Circuit symbol



Transistor viewed from base

manufacture in order to produce two rectifying junctions, that is two junctions which will allow current to pass more easily in one direction than the other. This construction is such that a small current in the base emitter junction can cause a relatively larger current to flow from emitter to collector. The device is therefore a current amplifier, the amplification factor of β being defined as

(change of collector current)/(change of base current)

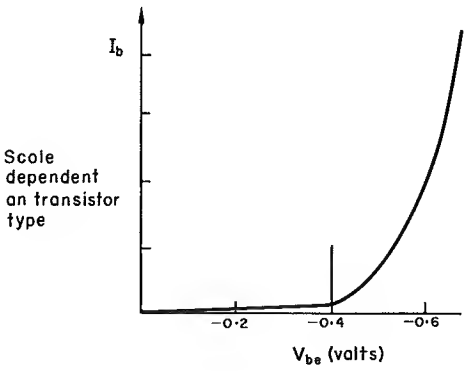
$$\beta = \Delta I_c / \Delta I_b$$

If, as is the case with silicon transistors, the leakage current in the collector emitter circuit is negligible when the base is open circuit, then

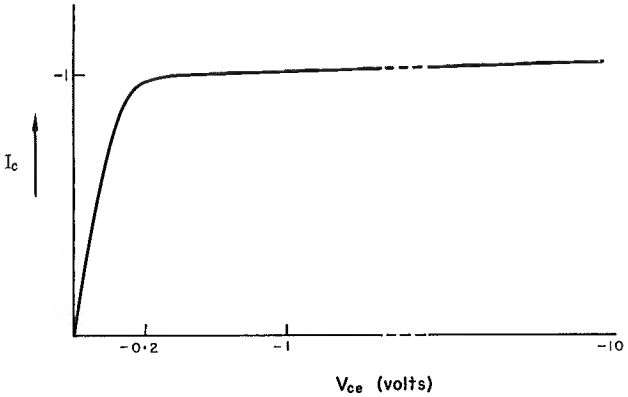
$$\beta = I_c / I_b$$

is approximately true. (This assumes β is constant for all values of I_c which in general is not true but is good enough for the derivations we will make.)

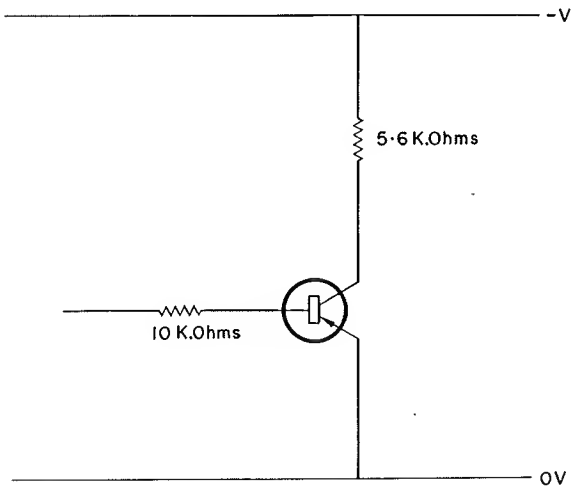
Although the above formulae are correct, the base voltage/base current characteristic is non linear. A typical graph of the base emitter voltage versus base emitter current is shown below.



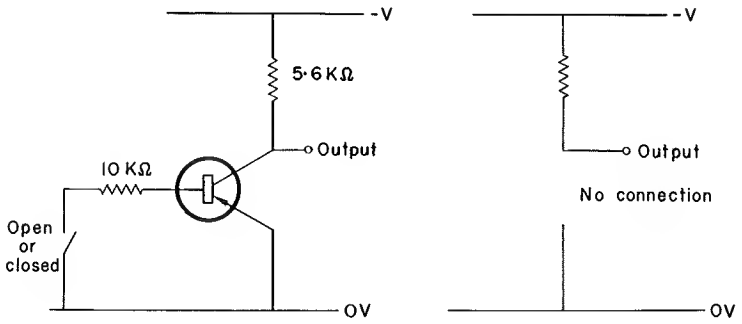
From this you can see that for a silicon transistor the base emitter voltage has got to be at least 0·4 volt before any base current will flow, and, no matter what base current does flow, will never exceed about 0·6 to 0·7 volt. The other characteristic that helps us in designing and using circuits to perform the NOR logic function is the graph of collector current I_c against collector emitter voltage Vce. This graph shows that the transistor has two approximately linear regions, one where the collector emitter voltage exceeds about 0·2 volt and the other below this figure.



You will notice that the voltages and current marked in these two diagrams are both negative, this is because the PNP transistor, like the OC200 we have used in the majority of the logic circuits requires, unlike the normal thermionic valve, a negative supply voltage. This is shown in the diagram of the NOR logic element.



Remembering the two previous diagrams it is then quite easy to work out just what will happen in this circuit. Firstly, if the input is not connected to anything, or is connected to the 0 volt line, then, since there is in both cases no base emitter voltage, there can be no base emitter current. Since we have also said that $\beta.I_b = I_c$ if I_b, the base current, is 0, then there can be no collector current and the transistor can be considered as an open switch, as shown in the diagram.



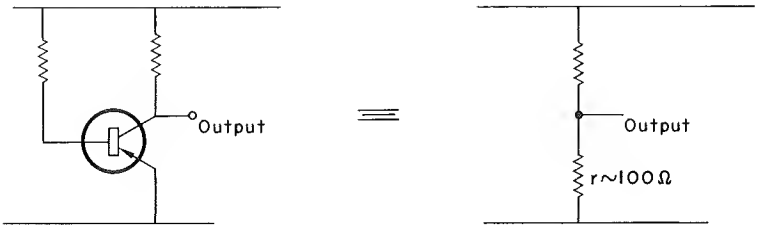
Thus the output voltage, when measured by a high resistance voltmeter, will be almost that of the supply voltage. It is important to remember that a high resistance voltmeter is needed here since any measuring instrument must draw some current through the 5·6 k. ohm resistor and, should current flow in this resistor, then there will be a voltage drop across it, as given by Ohm's Law ($V = I \times R$).

If we now connect the input to the negative supply, then current must flow since this supply voltage exceeds 0·5 volt. However, as we have shown in the first graph of I_b against *Vbe*, the base emitter voltage can never rise far above 0·5 volt. Therefore if we know the supply voltage, e.g. 10·5 volts, we then know the current which will flow in the 10 k. ohm input resistor. Since *Vbe* is 0·5 volt, the current, by Ohm's Law, is given by:

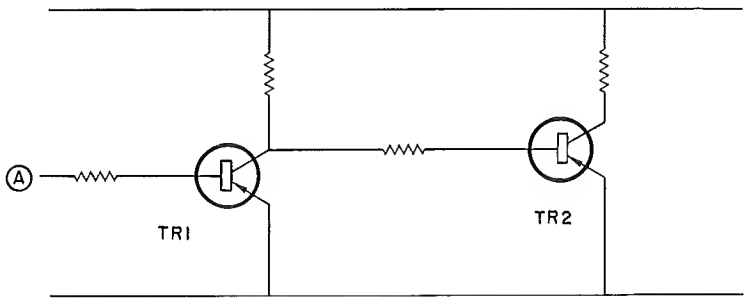
$$V\,\text{supply} - Vbe = \text{I} \times 10{,}000$$

This gives us a current through the 10 k. ohm resistor of 1 mA. This current, must, since there is no alternative path, flow through the base emitter junction of the transistor. A typical silicon transistor could have a current gain β of something greater than 10. If, in this example, we chose $\beta = 10$ we can then say what the collector current should be if $\beta \times I_b = I_c$. In this case we would have a collector

current of 10 mA. However, a simple Ohm's Law calculation on the 5·6 k. ohm resistor will show that in order to get 10 mA flowing in the collector emitter junction this current must flow through the 5·6 k. ohm resistor which would mean that there would be 56 volts across the latter resistor. The supply voltage, however, is only 10 volts so this is the maximum voltage there could be across the 5·6 k. ohm resistor. Therefore the maximum current through this resistor is 2 mA. Thus the equation $I_c = \beta I_b$ must be modified to $I_c \leqslant \beta \times I_b$. The inequality arises as the transistor collector emitter voltage changes from above 200 mV to below 200 mV. Thus when we connect the 10 k. ohm resistor on the base of the transistor to the negative supply the transistor conducts, a current of 2 mA flows in the 5·6 k. ohm resistor, the output voltage falls to almost zero and thus the transistor can now be thought of as a closed switch, since the small collector emitter voltage still present when the transistor is conducting is certainly less than 0·5 volt.



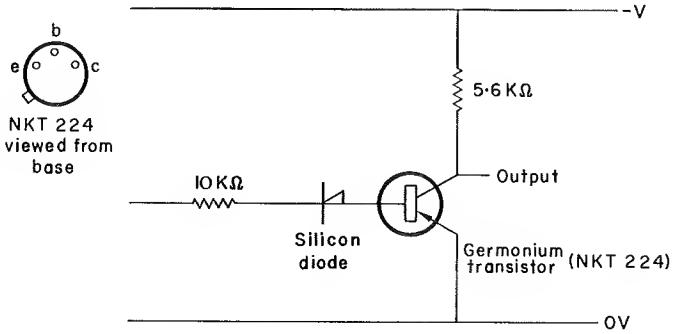
The second transistor, shown in the next diagram, will never conduct if the first transistor is conducting, i.e. point A connected to the power supply. When current flows in the collector emitter



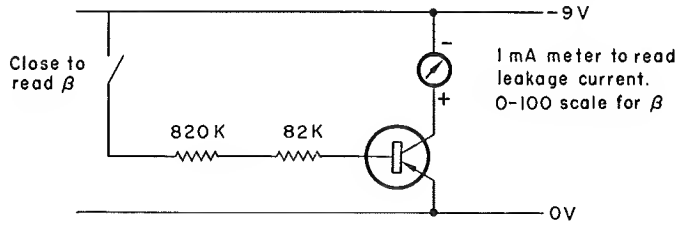
circuit of the transistor, the output becomes approximately 0 volts, the output is considered to be 'dead' or a logical '0' whilst if the transistor is not conducting, the output is at a large negative voltage then the output is considered 'live' or a logical '1'.

The previous paragraphs have only applied to silicon transistors in which there is negligible leakage current, that is negligible current in the collector emitter circuit when the base terminal is disconnected.

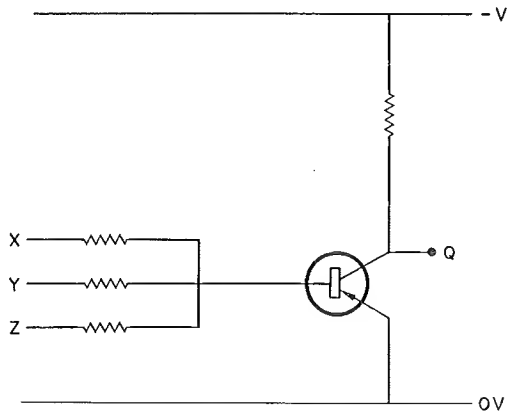
In order to construct logic units more cheaply germanium transistors can be used in the circuit providing that certain precautions are taken. Firstly one must include a silicon diode in series with the base of the transistor as shown in the figure. This is done to increase the base emitter voltage required before the germanium transistor conducts.



Secondly one must make sure that the germanium transistor chosen has low leakage current (less than 20 μ amps). Since if leakage current is present, the transistor no longer behaves as an open circuit switch when the base emitter voltage is less than 0·5 volts. Given that these conditions apply the germanium transistor with its associated silicon diode may replace directly the silicon transistor in the above discussion and circuits. A simple circuit for testing both the leakage current and the current gain of transistors is shown below so that any transistor may be selected for use in the logic circuits.



The circuits described previously show only one resistor on the base of each transistor. More than one resistor can be used and the circuit then operates so that if a logical '1' is applied to any of the points, X, Y, or Z, in the circuit below, the point Z assumes a logical '0'.



X	Y	Z	Q
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

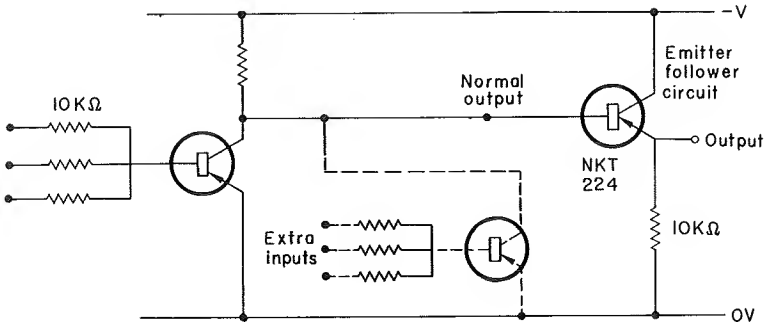
Truth table of NOR unit which shows the state at certain points.

This small unit is given the name of the NOR unit because the output Q is only 'live' if neither X NOR Y NOR Z is live. Since almost all the parts of our computer model will consist of these units linked in various ways, we will use a symbol for this circuit thus:

This symbol denotes a NOR unit with 3 inputs and 1 output, as shown—the resistor and transistor symbols are not shown and the −V and 0 volt lines are not inserted but must, of course, be present for the unit to function.

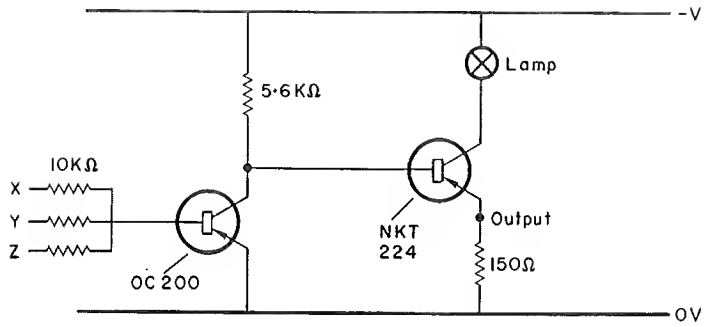
The number of inputs, called fan-in, and the number of other units supplied by the output point, called fan-out, can be varied but, as it stands, the number of inputs and outputs should not exceed three each, for the particular transistor used.

Failure may result if these figures are exceeded but if there is need to exceed the fan-in, then an extra transistor can be placed in parallel with the existing transistor while increase in fan-out needs an emitter follower amplifier. The figure below shows the transistor used to increase the fan-in and the normal output leading to an emitter follower.



At this point it will be realised that the state of the output can only be shown by using a voltmeter. This state can, of course, be shown by a lamp indicator but the circuit needs a transistor amplifier which will supply sufficient current to operate a lamp. The basic circuit, consumes approximately 2 mA while a lamp indicator will require a further 40 mA.

The following circuit shows the original NOR unit with the output fed to a second transistor. This second transistor, a Newmarket 224, will allow a large ratio of emitter-collector to emitter-base current. We need to use a value of about 40 for this and the chosen transistor is more than adequate.



The lamp must be one which will take only a small current (40 mA) and is an MES type radio panel bulb which we fitted into a normal batten type lampholder. The new output point from this NOR with indicator is from the emitter of the NKT 224. Again, this is live if neither X NOR Y NOR Z are live and notice that it follows the state of the collector of the OC200 because it is attached to the emitter of the transistor.

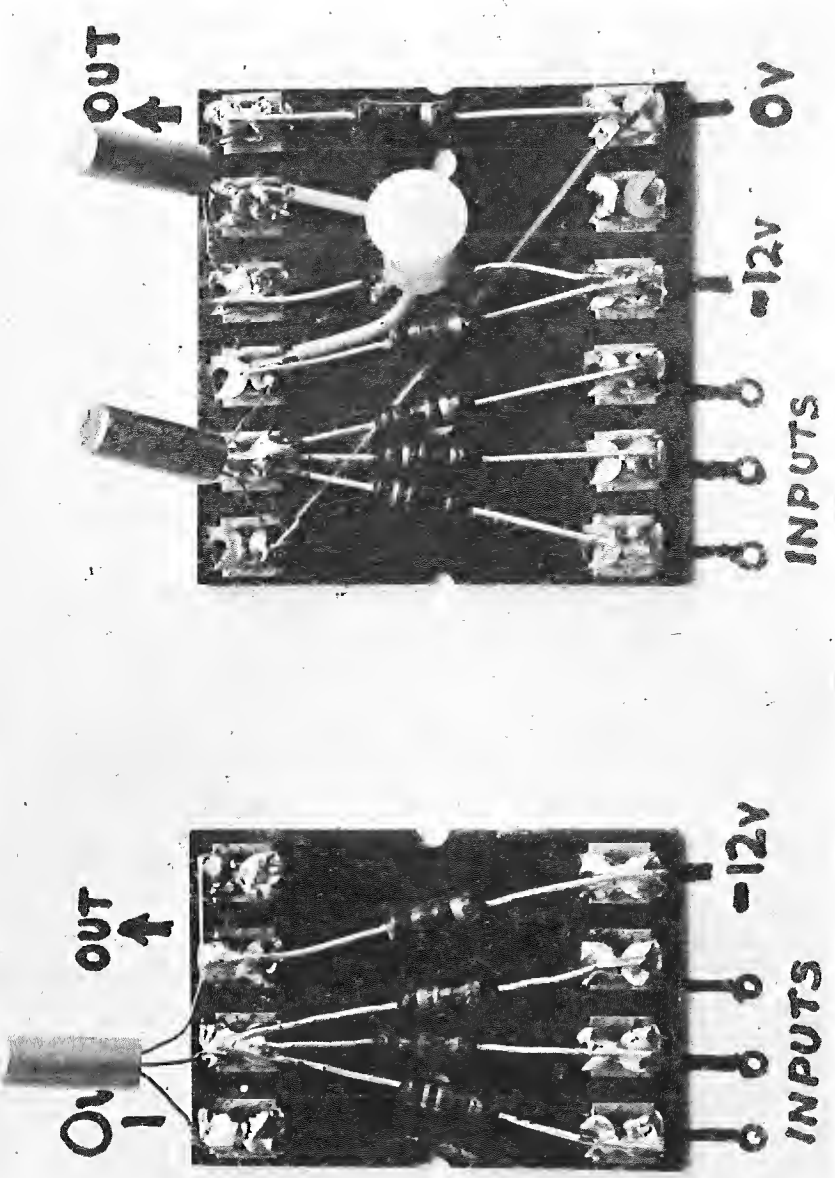
We distinguish between a NOR with a lamp, and one without, by an asterisk on the symbol, thus:

In our computer model, many NOR units will be used only a few of which will need an indicator—this is just as well because a NOR unit with a lamp uses 20 times as much current as one without.

The photograph on page 20 shows two NOR units, each with three inputs, the first without a lamp indicator and the second with the extra lamp and circuitry needed for it. The lamp is shown in the right-centre of the unit and would normally be mounted away from it. The output transistor in this circuit is a Mullard OC72 which is a suitable alternative to the NKT 224.

The output of the NOR unit can be expressed as a Boolean function of the inputs. This function, for a NOR unit with 3 inputs, labelled X, Y, and Z, is $X'.Y'.Z'$. This function indicates that the state of the output is a logical '1' if X is not '1', and Y is not '1' and Z is not '1'.

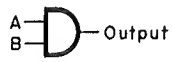
This output function is the same whether or not a lamp indicator is present. If only one input is present, say X, then the output would be



NOR Units.

simply X′ so that such a unit would merely invert the information received at X. Earlier books in the *Contemporary School Mathematics Series* have mentioned the complement of a binary number as being of use in subtraction, and we have here an electronic device (which will be discussed later in the book) which will perform this operation.

EXERCISE 1

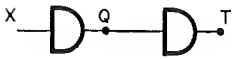
1. 

Complete the following table for the NOR unit in the diagram.

A	B	Output
0	0	
0	1	
1	0	
1	1	

Write down the Boolean function for the output.

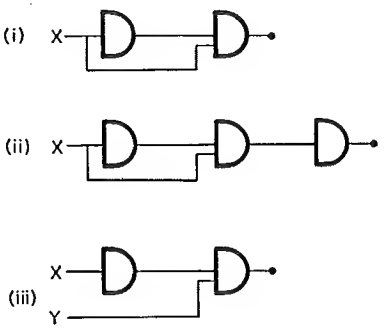
2. Write down the Boolean function for Q and then T and complete the table.



X	Q	T
0		
1		

3. Write down the Boolean function for T and see if you can design a simpler circuit than the one supplied which will produce the same output.

4. Write down the Boolean function for the output points in the following three cases:



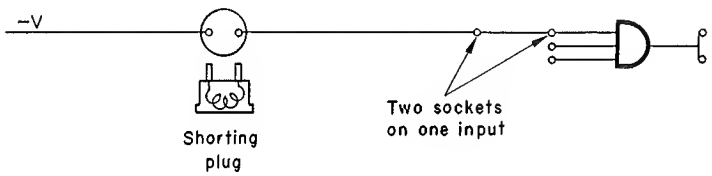
CHAPTER III

NOR Board Logic Circuits

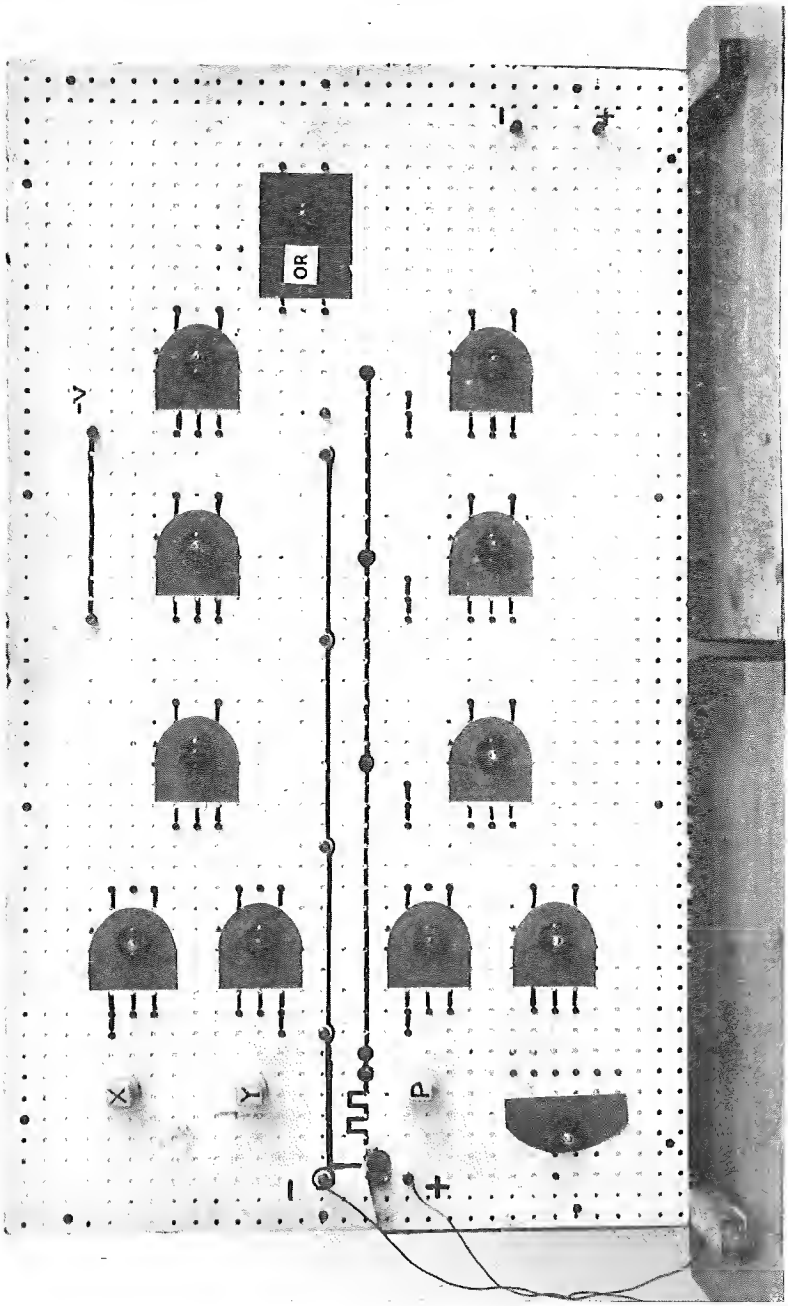
In order to demonstrate various circuits used in a computer a board was constructed on which were eleven NOR units as shown in the photograph. The symbols and lamp indicators are visible on the front of the board but all the electronic components are mounted on the reverse side. By interconnecting NOR units we can build up circuits which can be used to control operations inside the computer or can be used to solve logical problems. The addition of a few components to these units can produce the dynamic elements of the real computer.

Construction Details

The pegboard should be large enough to give adequate spacing of the units and still be easily handled. We chose a board 42 in. × 24 in. which was then painted white on the smooth surface. The NOR symbols, cut from card and stuck onto the front panel have the lamps mounted on top. Mini sockets, which will accept mini-plugs, are mounted at each input and output point—red sockets for input and black for output. Three units have one input with a double socket and a two-pin socket into which can be inserted a shorting plug, which of course, produces a logical '1' on this input.

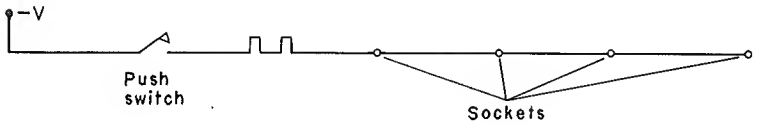


Terminal posts for connection to the positive (0V) and negative (−12 to −15V) points of a power supply are mounted at each end of the board and further terminal posts are connected to the negative



The NOR logic board.

post so that these points are permanently at a negative voltage. The lower line marked in the photograph, (page 24) is a line of sockets connected to a switch which, when pressed, produces a negative voltage on these sockets. This enables pulses of electricity to be produced manually—we call this the pulse line and it is indicated by the pulse symbol at the end of the line, thus:



3 groups of 3 sockets are arranged just below this pulse line and above the 3 in-line NOR units. These are useful for linking extra components and are isolated from everything else on the board.

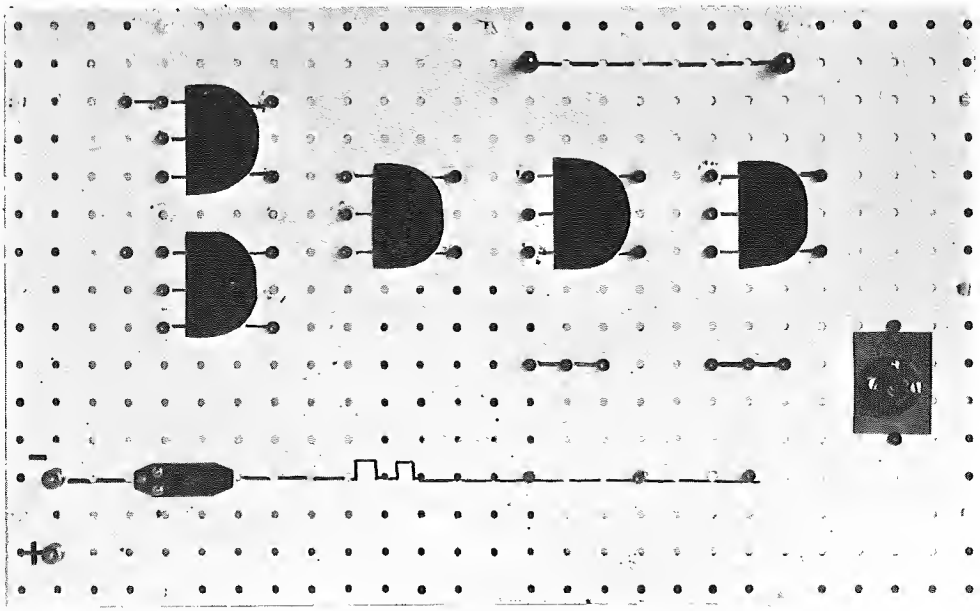
Points which must be remembered while constructing the board are:

1. See that your soldering iron is in good electrical condition. It should be small and have a small bit (about $\frac{1}{8}$ in.) suitable for transistor work—a meter test should be carried out to make sure that this bit is adequately insulated from the electricity supply and there is no electrical leak onto the bit.
2. The transistor leads should be gripped firmly while soldering with some good heat conductor to transfer heat away from the transistor. Some types of hair grips are satisfactory and leave hands free for other jobs.
3. Heat should be applied for a short time only.
4. Transistor leads should not be bent too close to the transistor case.
5. The ends of leads should not be mechanically linked to any tag so that, should the circuit need to be dismantled, it can be done without difficulty.
6. Try to arrange that the collector, base and emitter are mounted on adjacent tags.
7. Finally, see that you have good conditions under which to work —see that there is adequate lighting and that some device is available for holding the soldering iron in a safe position (when it is not in use). When the session is over see that all soldering irons are removed from mains sockets.

The board, as described, can be clearly seen by a class of, at least 35 students and, since no part of the circuitry is visible, anyone using

the board can concentrate on the logic problem and need not be concerned in any way with the technology of the circuit.

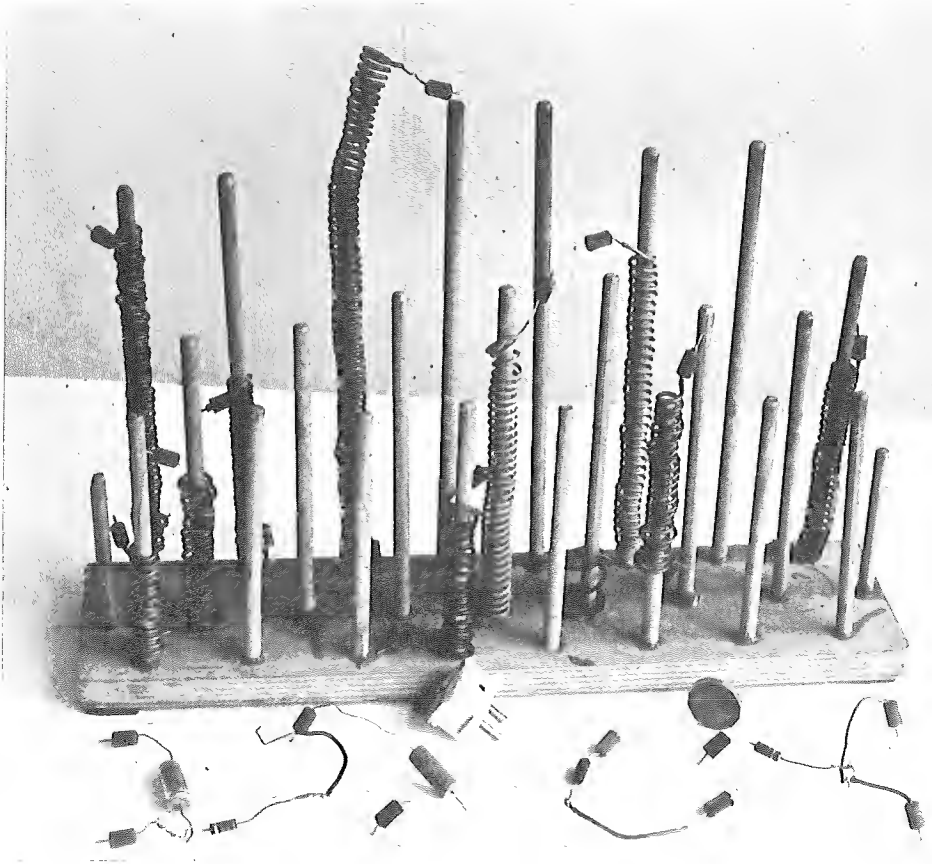
A more economical system is shown in the photograph below which is just 5 NOR units without indicators with one indicator remote from the units so that a connection from any NOR unit to the indicator unit will show the state of that unit. Two such boards would be almost equivalent to the first board and would enable two groups of students to work on logic circuits in place of only one.



Small version of NOR board.

Logic Gates

For this section linking wires are needed which should be single core wire, a number of different lengths of which should be prepared beforehand, each length with a mini-plug on each end which will fit the sockets on the board. The single core wire can be coiled and stored on posts on a special board resembling a test-tube rack and shown in the photograph opposite.

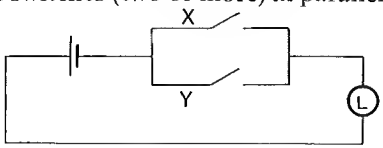


Components for use with the NOR board.

The longest length should be as long as the computer board and the shortest should be slightly in excess of the distance between two adjacent NOR units. Use a number of different coloured wires and decide on a colour code for lengths, such as red, green, blue, black for the short, medium, long, very long lengths. See that the colours stand out clearly from the background colour of the computer board.

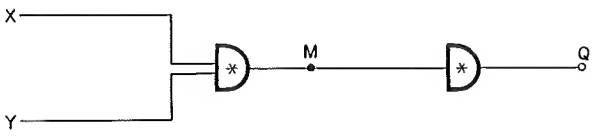
The 'OR' Gate

Earlier books in the *Contemporary School Mathematics Series* show this gate with switches (two or more) in parallel thus:



If X *or* Y is closed then L (lamp) will light.

Now consider the following circuit



A signal (logical '1') applied at X *or* Y will cause output Q to be live (logical '1'). When X, or Y (or both) are live, M is dead and Q is therefore live.

The truth table for this is

X	Y	Q
0	0	0
0	1	1
1	0	1
1	1	1

The Boolean functions are

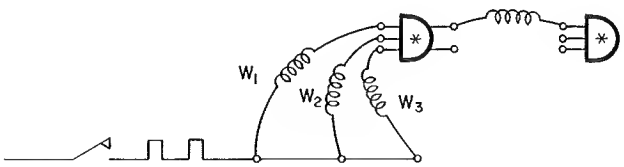
at M $X'.Y'$

at Q $(X'.Y')'$ which, by De Morgan's Laws

$= (X')' + (Y')' = X + Y$

We are not limited to two inputs to this unit—more can be added (provided we bear in mind the fan-in specifications of the circuit).

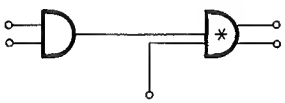
A three input OR gate can now be installed on the board. A short link wire and three longer link wires W_1, W_2 and W_3 are needed.



Connect the NOR board to the power unit. All NOR unit lamps should be on. Insert a link wire from the output of one NOR unit to the input of an adjacent unit. The second unit should now switch off because the link wire is live. Insert W_1 and press the pulse line switch. Repeat this with W_2; W_3, W_1 and W_2, W_1 and W_3, W_2 and W_3, W_1 and W_2 and W_3 inserted. Fill in the following table by denoting the presence of a link wire by 1 and its absence by 0, the on and off states of the lights by 1 and 0 respectively.

W_1	W_2	W_3	1st Lamp	2nd Lamp
0	0	0		
0	0	1		

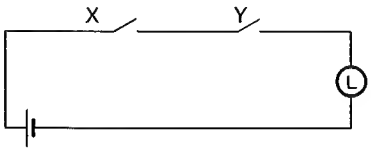
This unit is used so frequently that we inserted one on the board as a permanent feature. The rectangular block at the right hand side is such a unit with the indicator lamp on the final NOR unit and 2 inputs to the gate with one to the second NOR unit thus:



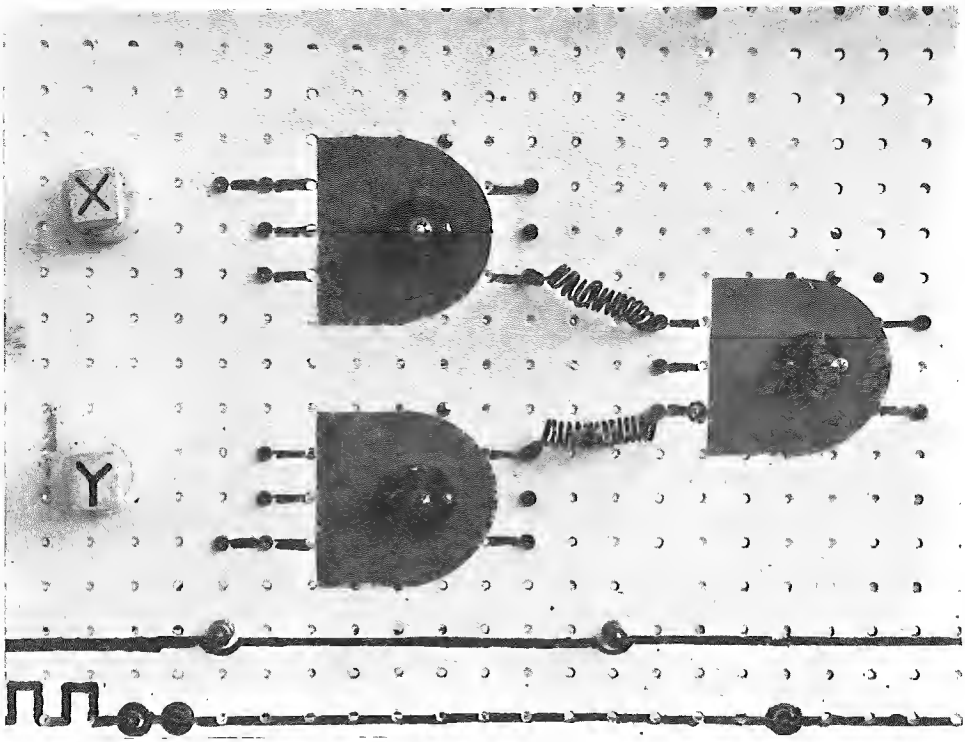
In future an empty board, when switched on should show all lamps on except this one.

'AND' Gate

Referring again to the normal switch AND gate we have a series arrangement

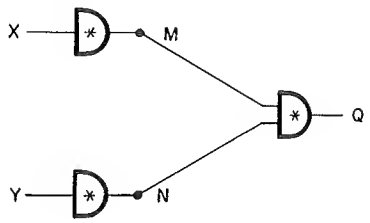


so that X *and* Y must be operated for L to be on. A NOR logic arrangement can be assembled to perform the same function and to be very much more practical in a computer.



AND gate arranged on NOR board.

Consider the circuit:



A signal (logical 1) applied at X *AND* Y will cause output Q to be live (logical '1'). When X, or Y but not both are live then M or N is live thus holding Q off. Only when X and Y are live are both inputs to the final unit dead, so allowing Q to be live.

The truth table for this

X	Y	Q
0	0	0
0	1	0
1	0	0
1	1	1

while at M and N

M	N
1	1
1	0
0	1
0	0

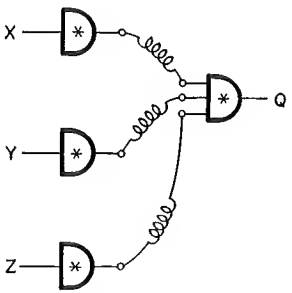
The Boolean functions are

at M, X'

at N, Y'

at Q, $(X')'.(Y')' = X.Y$

Again we are not limited to 2 inputs and we shall now arrange a 3 input AND gate on the NOR board. For this we need 3 link wires, 3 two-pin shorting plugs for 3 sockets on the board.



For this experiment we will use the sockets mounted on the inputs to the three left hand NOR units. These plugs can be labelled X, Y and Z. Three link wires connect the outputs of these three NOR units to the 3 inputs of the final NOR unit. Notice that, on insertion of plug X the lamp on that NOR unit is extinguished, similarly for Y and Z.

Now try the eight possible arrangements of X, Y and Z in and out of the sockets. Observe the output Q and complete the eight lines of the table below:

X	Y	Z	Q
0	0	0	
0	0	1	
0	1	0	

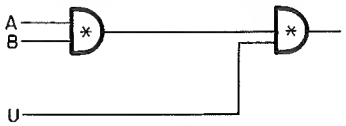
and for M, N, K

M	N	K

Inhibition

Both the OR and AND gates can be inhibited if desired. That is, we can completely cancel the output by applying one particular input.

Consider the OR gate with an extra input fed to the last NOR unit.



If U had not been attached then the whole gate would operate as a normal 2 input gate. However if U is present and live (logical '1')

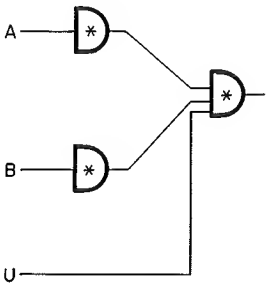
then the output will be '0' no matter what is the state at A or B. The output might well be defined as A OR B UNLESS U and a truth table derived for this

A	B	U	OUTPUT	
0	0	0	0	normal 'OR' gate operation
0	1	0	1	
1	0	0	1	
1	1	0	1	
0	0	1	0	Complete lack of output due to presence of U
0	1	1	0	
1	0	1	0	
1	1	1	0	

The rectangular OR unit on the right hand side of the NOR board is fitted with this inhibitor.

You may imagine statements being made which could be translated into NOR circuits. For example, in the last circuit A, B and U could represent America, Britain and the U.S.S.R. and we could have the following statement:— 'Agreement will be reached if America or Britain is present at the conference unless the U.S.S.R. is present'. This inhibition is just like a veto in the United Nations.

The AND gate with inhibition would look like



The output is live if A AND B UNLESS U—in our last example both America AND Britain would have to be present for agreement to be reached.

The reader should build these circuits on the NOR Board and fill in the truth table for the last example and compare the table with the output states on the board.

Exclusive or (or else)

It will be realised that the word OR is sometimes rather ambiguous. Our previous examples allow the case of both inputs together being a valid state for an output to be present. However, there are occasions when the two together are not allowed. Take the two statements

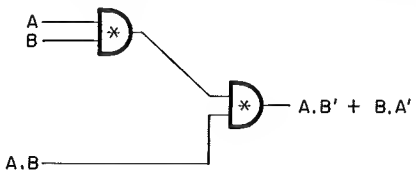
1. I will go to the theatre provided Agatha *or* Brenda will give me the money.
2. I will marry provided Agatha *or* Brenda will be my wife.

In (1) the case of both A and B giving money is allowed but in case (2) we do not want this. It is usual to take OR as meaning case (1) while we add the word 'else' if we wish to discount the two together, thus (2) would be written 'I will marry provided Agatha *or else* Brenda will be my wife'.

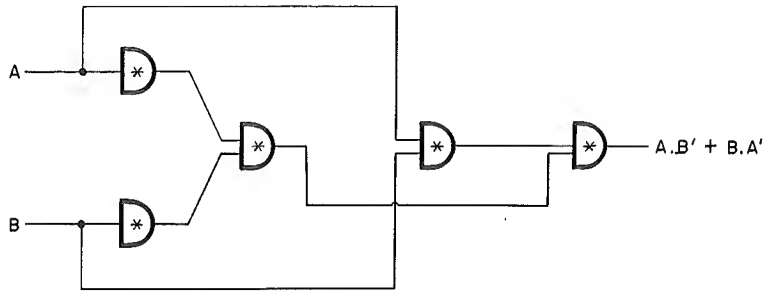
A truth table for statement (2) would be

A	B	M
0	0	0
0	1	1
1	0	1
1	1	0

The Boolean expression must show that we can have (A and not B) OR (B and not A) written $A.B' + B.A'$. In set theory this is referred to as the symmetric difference of the two sets A and B and can also be written $A \nabla B$. The circuit would be a normal OR gate inhibited by A.B thus



The A.B input must be obtained from A and B so that the complete circuit is



You should be able to arrange the complete circuit on the top half of the NOR Board and use the two shorting plugs which can be labelled A and B.

Implication

Take a boy, Andrew, and a girl Barbara. If a dance is being held in the local dance hall we could have any one of four cases arising concerning the attendance at the dance of these two people. They can be laid out in table form in which 1 denotes presence and 0 absence.

A	B	
0	0	Both absent
0	1	A absent, B present
1	0	A present, B absent
1	1	Both present

However we could make the following statement:
'The presence of Andrew at the dance implies the presence of Barbara' written in logical notation as $A \Rightarrow B$. This immediately cuts down the 4 cases listed above.

We know that Barbara is present if we see Andrew and we know, from this, that the case of Andrew's presence and Barbara's absence is not now a possibility. Barbara without Andrew, and the case of

both absent are still possibilities since they do not violate the condition laid down. We can list these in a truth table for implication as follows:

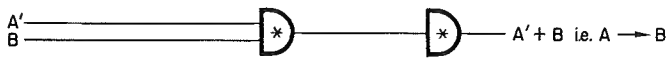
A	B	A ⇒ B
0	0	1
0	1	1
1	0	0
1	1	1

'0' denotes 'not possible'

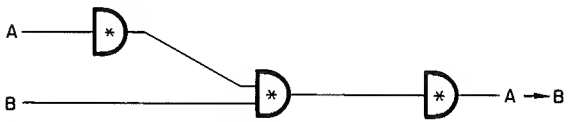
If we next examine a truth table for A′ + B we see that the column A′ + B is identical to A ⇒ B.

A	A′	B	A′ + B
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1

Thus a NOR logic circuit for A′ + B could be used for this statement thus



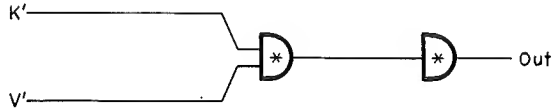
or better as



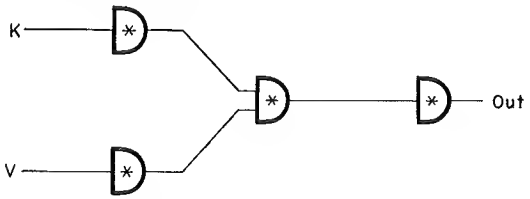
where A is entered in its direct form.

This can now be arranged on the NOR board and the full range of possibilities investigated to see if the end product compares with the table provided.

Here is a similar statement with an extra inversion in it: 'If you drink you must not drive'.
Let K denote drinking and V denote driving.
The above statement can be written $K \Rightarrow V'$
The equivalent Boolean function $K' + V'$.
The NOR circuit diagram



The full diagram with direct inputs



K	V	OUT	
0	0	1	Allowed by Law
0	1	1	,, ,, ,,
1	0	1	,, ,, ,,
1	1	0	Not allowed by Law

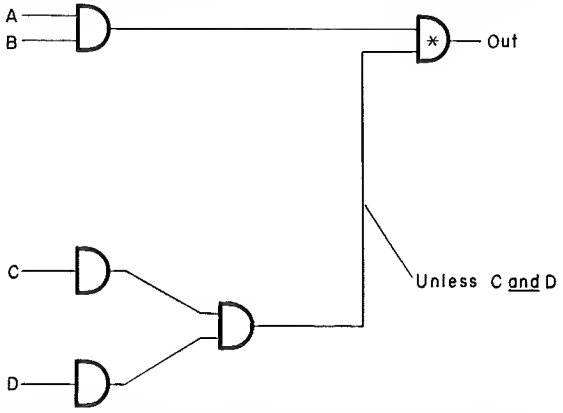
The understanding of this type of statement is very important—so many people misuse it in everyday conversation.

It should now be clear that statements can be expressed in NOR circuitry and that we may be able to arrive at certain conclusions if a set of statements are made. These conclusions, instead of being worked from first principles could be investigated on the NOR board by going through all the possibilities and observing the final output lamp which would be on for a satisfactory set.

Example 1

I will go to the meeting tonight if Arthur or Bert come with me unless Clarence and David are present.

The Arthur or Bert part is straightforward but 'unless' implies an inhibition, in this case based on Clarence and David together



With 4 inputs we have 2^4 different arrangements which can be gone through methodically to find which, if any, of the arrangements will cause the lamp to light. The complete truth table is as follows:

A	B	C	D	A + B	C.D	Output	Will I go?
0	0	0	0	0	0	0	No
0	1	0	0	1	0	1	Yes
1	0	0	0	1	0	1	Yes
1	1	0	0	1	0	1	Yes
0	0	1	0	0	0	0	No
0	1	1	0	1	0	1	Yes
1	0	1	0	1	0	1	Yes
1	1	1	0	1	0	1	Yes
0	0	0	1	0	0	0	No
0	1	0	1	1	0	1	Yes
1	0	0	1	1	0	1	Yes
1	1	0	1	1	0	1	Yes
0	0	1	1	0	1	0	No
0	1	1	1	1	1	0	No
1	0	1	1	1	1	0	No
1	1	1	1	1	1	0	No

Naturally testing every possibility is likely to prove tedious even in this problem with only 4 variables, but one with say 7 or more, i.e. 2^7 possibilities or more, could be a real trouble. Later it will be shown how we can test all these possibilities with our model computer at a rate in excess of 1,000 tests per second.

Example 2

Father will allow his son to apply for a driving licence provided he has reached the age of 17, has the fifteen shilling fee and can get the use of his brother's or a driving school car.

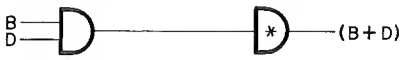
Let A represent age over 17.

Let F represent the fee.

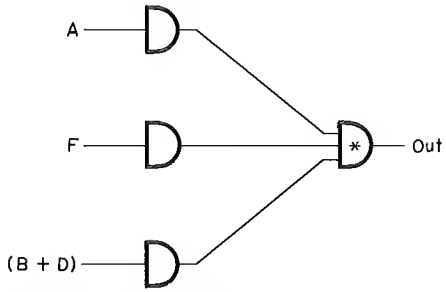
Let B represent brother's car.

Let D represent driving school car.

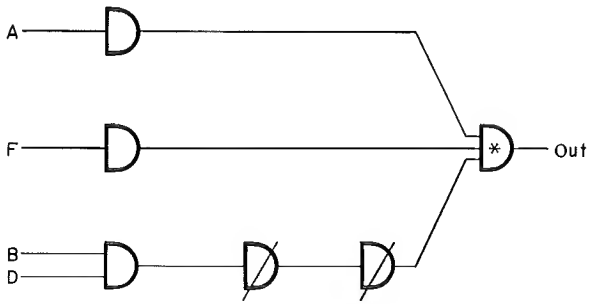
The circuit gate for brother's car or driving school car



The circuit for the main AND statements



There is however, often a simplification which can be carried out when circuits are combined. Two NOR units in series can be eliminated as it is really a double inversion. These are shown crossed out in the diagram:



which is quite an economy on NOR units.

You should now set up this circuit on the board, make out the truth table and determine the Boolean function of the output.

Example 3

A man decides that he will only marry a girl who will satisfy any of the following conditions:

1. She is pretty.
2. She is a soccer fan and has a rich father.
3. She is a golf player and has a rich father.

Construct a circuit which will give specifications of a suitable bride.

Let P represent pretty.

S ,, a soccer fan.

G ,, a golf player.

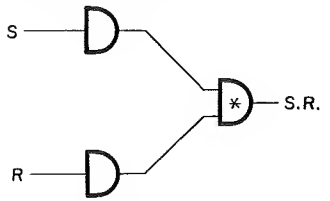
R ,, a rich father.

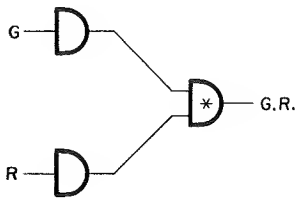
The whole set of conditions may be written:

$P + (S.R) + (G.R)$.

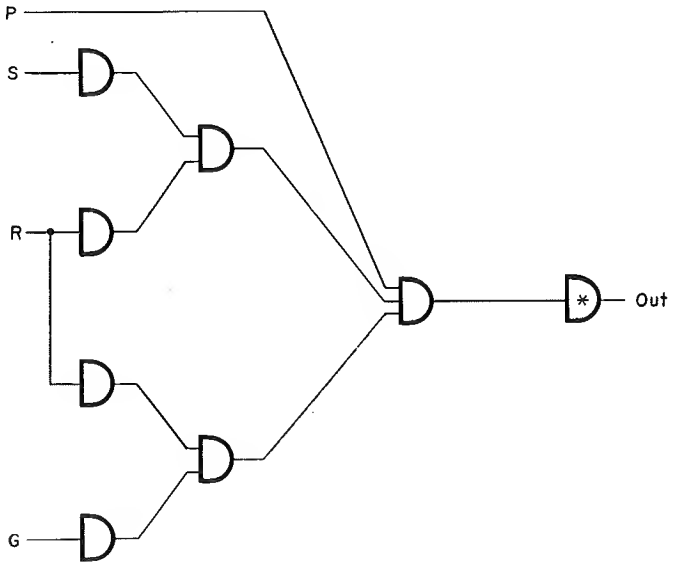
Thus circuits for P, (S.R), (G.R) can be fed into an OR gate.

For S.R and G.R we have



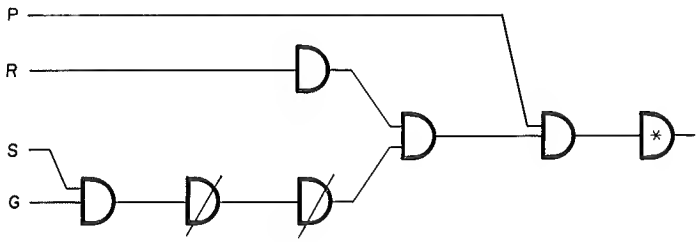


and the whole circuit therefore becomes



which requires 8 NOR units. However the first expression can be simplified by using the distributive law so that

$P + (S.R) + (G.R) = P + R.(S + G)$ giving



(notice the two cancelled NOR units).

This circuit can again be constructed. We have 3 shorting plugs, the fourth variable can be a wire from the switch line to the input of one of the units or a fourth socket could be added to the board. This is one advantage of building the board—extra units or components can be added if you wish without a great deal of expense.

Again truth tables and a list of satisfactory answers should be given.

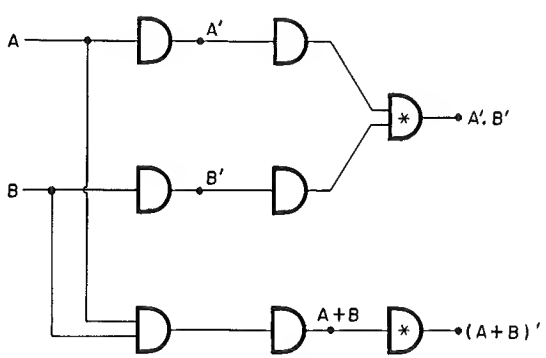
Example 4

De Morgan's Laws

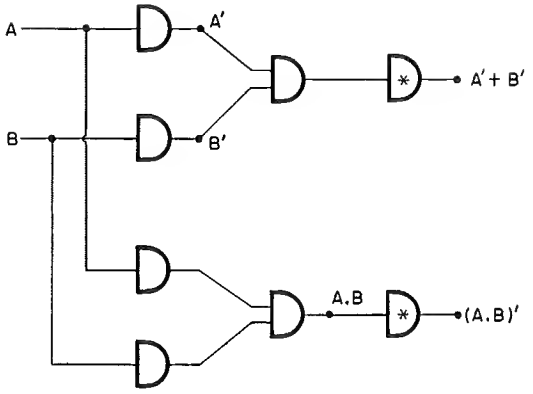
1. $(A + B)' = A'.B'$
2. $(A.B)' \quad = A' + B'$

We can set up circuits to show each of the above laws.

(1)



(2)



In diagram (1) observe that the outputs $A'.B'$ and $(A + B)$ are equivalent.
In diagram (2) observe that the outputs $(A' + B')$ and $(A.B)'$ are equivalent.

EXERCISE 2

Design circuits for the following:

1. A meeting of the Committee will take place on the 1st day of every month provided the Treasurer and Secretary can attend unless the 1st day of the month is a Sunday.

2. The same as No. 1 except that for Sunday read Sunday or Wednesday.

3. You can take a course at this College provided you have passed examinations in Maths and English or Science and French.

4. As for No. 3 but add 'unless you are in poor health'.

5. The safe can be opened by the Manager and Cashier or the Cashier and a Director unless the Burglar Alarm is switched on.

6. A baby is to be born into a certain family and heredity factors predict that if it has blue eyes it will also have curly hair and that it will have either webbed feet or else large ears. (Remember blue eyes implies curly hair: written $B \Rightarrow C$ or $B' + C$.)

7. I have three friends and I intend to take all or some of them on holiday to either Austria or Germany, but Bill won't go with Claude and Eric won't go to Germany while Austria will not permit entry of Bill. Where shall I go and with whom?

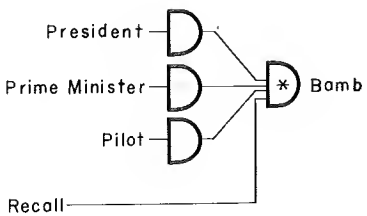
8. Four suspects arrive at a Police Station and it is known that at least one of them is involved in the crime, but that ALF and DEFTY

are not both guilty together. Also it is known that if
ALF is guilty then so is CURLY and if
BENDY is guilty then DEFTY is not.
Make out a list of the possible guilty groups—see if you can add further statements which will narrow the field.

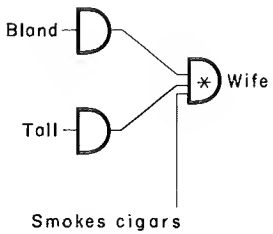
9. An interviewing panel will accept for employment any candidate who has 2 out of the following 3 qualities:
(*a*) Good qualifications.
(*b*) Well-dressed.
(*c*) Outstanding personality.
Design a circuit to represent this, and then adapt the circuit to deal with the further statement
(*d*) Unless he is over 30 years of age.

The following diagrams may suggest certain problems to you—if so state them.

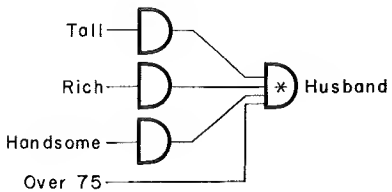
10.



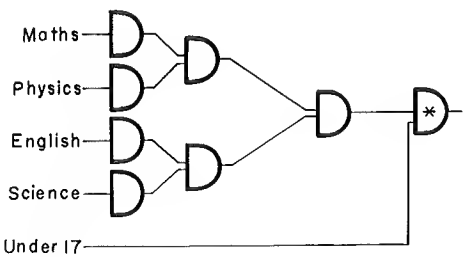
11.



12.



13.



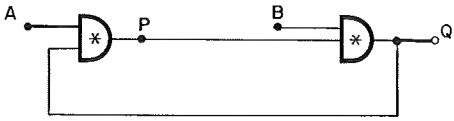
CHAPTER IV

Logic to Arithmetic

The NOR logic circuits can be combined to do simple arithmetic, however, before we discuss these circuits, there are a few other simple arrangements which will be useful.

Memory Cell

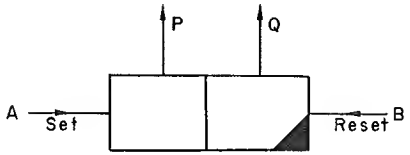
This cell, often referred to as the bistable or flip-flop, has two states as suggested by the name. Two NOR units are involved thus:



This is simply two NOR gates with the final output fed back to one of the inputs of the other. A and B are inputs to the first and second NOR units respectively.

The outputs P and Q from the first and second NOR units cannot be in the same state. If P = 0 then Q = 1 and if P = 1 then Q = 0. In this last state, lamp No. 2 is off and if we look only at this lamp, that is output Q, then we can say that, in this state, the cell is storing '0'. When in the other state it is storing '1'. Clearly the first lamp need not be present in the circuit and such a circuit can be built up on the NOR board using the OR gate on the right side of the board and linking one output to one input point. Since this unit has only one lamp it is more obviously storing 0 or 1. To change the state from 0 to 1, we need only apply a '1' condition to A, Q will then assume a '1' state and will keep this state whether the applied condition is retained or not. In fact the applied condition need only last for about 0·0002 seconds in this particular circuit. To reset the cell we need to apply a '1' condition to B; naturally the application at A must, by

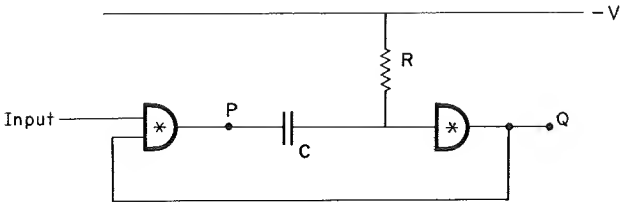
now, have been discontinued. Since this cell will be used often we have a symbol to replace the circuit above.



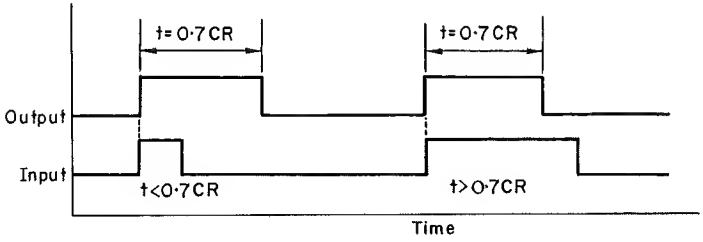
The shading in the box denotes that the unit has one lamp indicator which is on after a set operation. In the set state the line Q will be live and the line P dead.

Monostable or Delay Circuit

The monostable is two NOR units arranged in a similar manner to the bistable but with additional circuitry to cause one particular side to be on in the quiescent state.



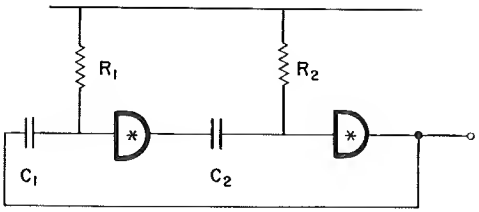
The extra components are the resistor R and the capacitor C. As it stands the first lamp will be on so that P = 1, Q = 0 which is the stable state of this unit. An application of a live signal to the input causes Q to assume the '1' state for a length of time, which is dependent on C and R, before resuming the '0' state. This time $t = 0{\cdot}7CR$ (R in ohms and C in farads) is not in any way dependent on the length of the input signal. The signal can be for a shorter or longer time than t. We can represent this in diagram form, this kind of diagram is very common in computer work and shows a signal applied for a length of time and referred to, in future, as a pulse.



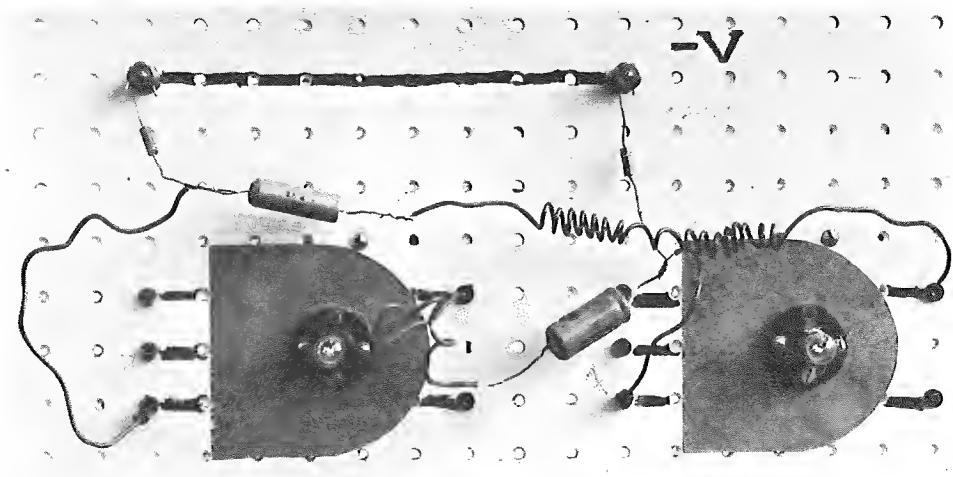
The diagram (foot of page 45) shows first an input pulse applied for a shorter time than the output signal, followed by a second pulse longer than the ouput signal. Although this is called a delay circuit it does not delay the start of the output pulse. The start must coincide with the start of the input pulse and the end may be delayed to your specification. This gives us a useful way of 'tailoring' pulses.

Multivibrator or Pulse Clock

By adding extra components it is now possible to remove the stability of the last unit and cause continuous oscillations:



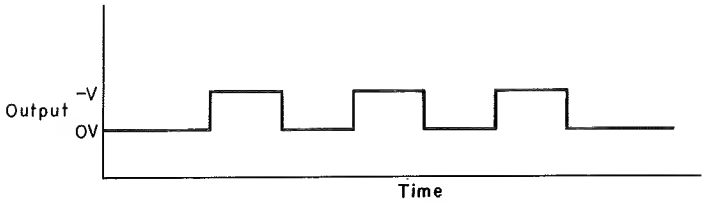
We have really added the same components between the output of the second NOR and the input of the first NOR as we have already added between the output of the first and input of the second NOR unit. This causes continuous flashing, at speeds which are determined by the C and R values. If $C_1 = C_2$ and $R_1 = R_2$ then the time period



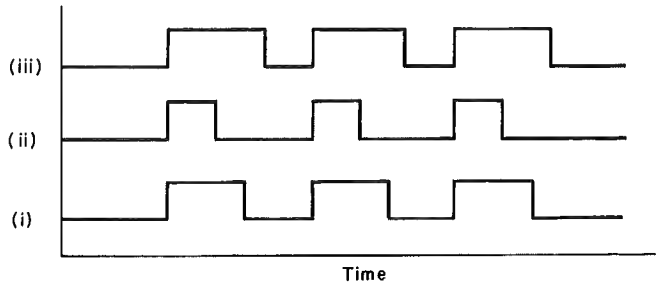
Pulse Clock mounted on NOR board.

of one oscillation is approximately $0{\cdot}7C_1R_1$ and each lamp is off and on for the same length of time. The relative times of the on and off conditions can be altered by making $C_1 \neq C_2$ or $R_1 \neq R_2$. With $R_1 = R_2 = 33$ k. ohms and $C_1 = C_2 = 100$ μF we can see the oscillations quite clearly since the time period is approximately 2 seconds. A change in the values will produce higher or lower frequencies as desired but the time period quoted is very satisfactory for demonstrations. 16 μF capacitors give quite a useful speed for a number of experiments to be described later while speeds up to 5 k/c (5000 cycles per second) are possible. If components are changed while the pulse clock is switched on there is a possibility of the unit stopping but it can be restarted by switching the supply voltage off and on again.

A diagram showing the output of this clock would look like:



These pulses will be used in the computer in very much the same way as the ball bearings were used in the ball-bearing machine. The shape of these waves are said to be square since both the leading and trailing edges are perpendicular to the time axis. This sudden rise and fall in voltage is not common in electrical work but in computer work it is most desirable that it should be so. The diagram below shows the form of the output obtained when (i) $C_1 = C_2$ (ii) C_1 is greater than C_2 (iii) C_1 is less than C_2.

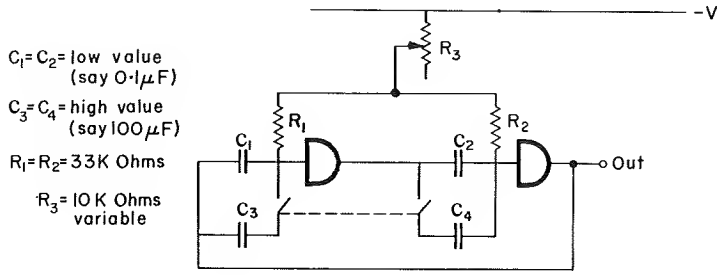


In all cases the value of R should be such that

$$10 \text{ k. ohms} \leqslant R \leqslant 50 \text{ k. ohms}$$

It is also recommended that C_1 and R_1 should not differ greatly from C_2 and R_2 respectively.

It is now advisable to build this unit on the NOR board and familiarise yourself with it by varying C and R values and observing the effects. Two terminal posts mounted above the top two right-hand NOR units and connected to −V will facilitate this construction. Since a pulse clock is needed in other models later, it is advisable to build one with only one indicator lamp and which also has each capacitor mounted between two terminal posts so that they can be quickly changed. Alternatively, a switch can be installed which will switch in low or high value capacitors for high or low speeds. The diagram below shows a suitable system for switching which includes an extra variable resistance which can be used for fine adjustment if required.



Although we have no real need to know the exact speed of this clock for the main computer model, its speed can be very accurately determined as we shall see later. With frequencies of 1 cycle or 1 kilocycle per second we can see clearly each operation in turn or the speed with which a number of operations can be performed.

The following demonstrations will help you to see how the pulse clock can be controlled.

Demonstration No. 1

To show methods of controlling the output from a Pulse Clock.

Apparatus required

1 NOR Board
Power Supply

Two Capacitors (100 μF)
Two Resistors (33 k. ohms)
Link Wires

The pulse clock is the heart of the computer and its pulses will be directed to various parts of the model computer.

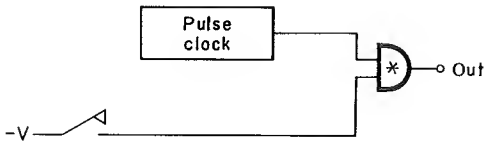
We will now show how, without stopping the clock, the pulses can be permitted or prevented from flowing by means of simple networks.

The pulse clock should be built up on the board using the 100 μF capacitors and 33 k. ohm resistors which will give a slow pulse rate. This clock will now oscillate continuously and we will control the flow in three different ways:

1. Using a NOR element and a manually operated switch. This system will invert the output from the clock.

2. Using an OR gate and a manually operated switch which does not invert the output from the clock.

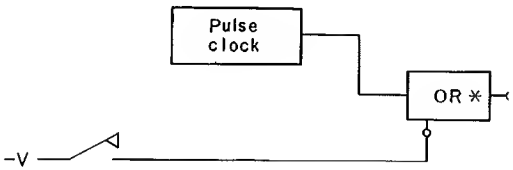
3. Using an electronic switch, or memory cell, to control the output.



(i) Choose a convenient NOR unit and feed the output of the clock to one input of the unit and the pulse line to the other.

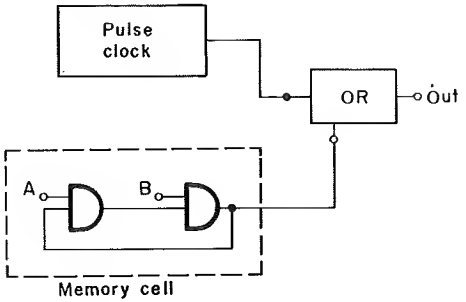
Notice that the output of the NOR unit is the inverse of the output of the pulse clock. Thus a stream of pulses can be obtained from this unit. If the switch on the pulse line is depressed then this flow ceases although the clock is still oscillating. You can, therefore, by manipulating the switch, control the pulse flow from the clock.

(ii) The diagram shows the set-up for this demonstration in which the clock is connected to the OR gate which has its inhibition point connected to the pulse line.



The output of the OR gate is now in step with the output of the clock and is controlled by the switch. Depressing the switch causes the flow to cease. This method has the advantage of copying the output of the clock but requires one more NOR unit than the last case.

(iii) Construct a memory cell on the two NOR units directly below the pulse clock. The output of one of the NOR units should be connected to the inhibit point of the OR unit—if this output point is live the output of the OR gate will be dead. If the output point is dead the output of the OR gate will copy the output of the clock. To cause pulse flow from the output, touch point B on memory cell. To stop the pulse flow touch point A on memory cell which causes the lead to the inhibit point to be live.



This has shown how an electronic device, the memory cell, has controlled the pulse flow. Information in the form of a single pulse at A or B can prevent or permit pulse flow from the output of the OR gate.

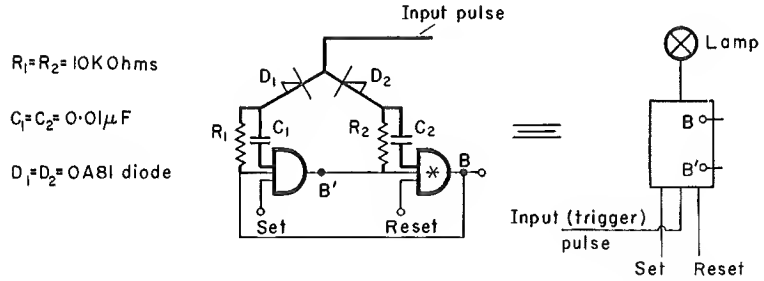
Question

See if you can devise a circuit to control the pulse flow from the output of an AND gate in place of the OR gate. Can you say why the OR gate with inhibit is to be preferred to the AND gate?

Scale of Two

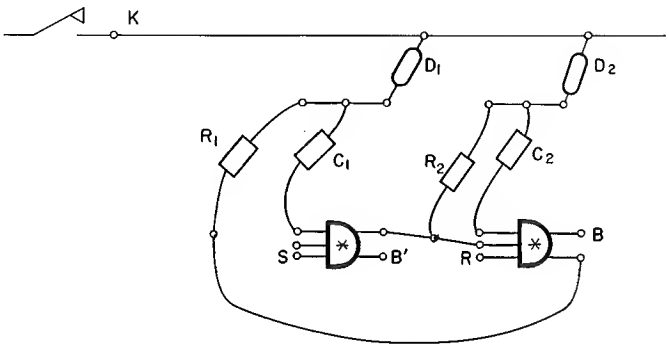
In the bistable circuit we had a circuit which could be in one of two states which were decided by inputs at one or other of the two NOR units. We can extend this so that a single input will change the state. This simply means that a single signal will be directed to the NOR unit which will affect the change. If the output state is 1, the next pulse to the unit will change it to 0 and if the output state is 0 then the next pulse will change it to 1.

This operation is carried out by adding a routing circuit to the basic bistable circuit which directs the input signal to the NOR unit which needs it. The diagram below shows the complete scale of two unit—you should be able to pick out the routing circuit leading from the input down to the two NOR units, the symbol to represent this unit, in future, is also supplied.



The set and reset points are still available for a change to a desired state, while a single pulse applied to the input point will cause a change to the opposite state. The diodes allow current flow in the direction of the arrow and the actual diode has a red spot which is to be taken as the head of the arrow. A number of these units will need to be built for future use and only the second lamp need be installed so that B is in the '1' state, and B′ in the '0' state when the lamp is on.

The scale of two can now be built up on the lower part of the NOR board as shown in the following diagram:



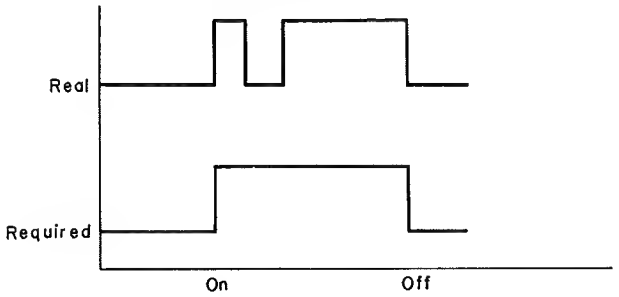
Having arranged this circuit, touch S and R to set or reset the unit and so check that the bistable is working correctly. Now press the switch a number of times and watch the controlled oscillation of the unit. Next use a slow pulse clock which can be built above this unit

and feed the output of the clock into socket K so that pulses are flowing into the scale of two unit. Observe that the unit is oscillating at half the speed of the clock. For this reason it is sometimes referred to as a 'divide by two' circuit. You will observe that you have here an electronic analogy of the flip-flop on the ball-bearing machine. The following table will summarise the effects of applying pulses at various points.

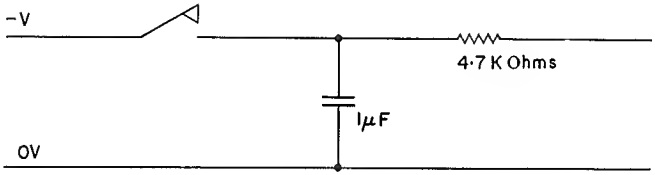
Existing State	Pulse applied at	New State
Lamp ON, B=1, B′=0	Reset	Lamp OFF, B=0, B′=1
	Set	No change
	Trigger (Input)	Change to lamp OFF B=0, B′=1
Lamp OFF, B=0, B′=1	Reset	No Change
	Set	Lamp ON, B=1, B′=0
	Trigger	Change to Lamp ON, B=1, B′=0

Note on Mechanical Switches

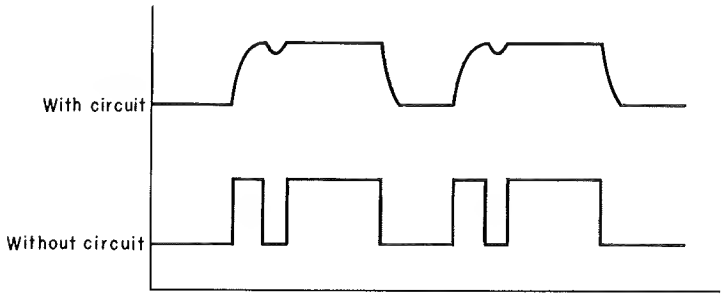
When a switch closes, although it is very difficult to see, the contacts close and then rebound open again, this occurring sometimes a number of times before the final closed condition is reached. The scale of two unit will work so very quickly that it will react to each of these makes and breaks of contact. The diagram below shows what often happens and what we would rather have happen.



The effect of these bounces can be countered by a simple capacitor resistance network which, in effect, cuts out the small gap between the pulses that would otherwise occur. The circuit below is effective and allows a slow decay of the pulse. For this reason the capacitor must not be too large in case the real gaps between pulses disappear.



The effect of the pulse form is shown here:



The top wave form shows the decay action on the pulse which means that the small initial pulse does not decay sufficiently while the bounce is taking place, but on the other hand decays sufficiently quickly to disappear before the next pulse arrives.

Scale of two elements are the basic elements of counters and are very common in the real computer, not only for counting but also for controlling sequential operations. The binary, or two state, system is used because it is so easy to handle. The denary system would require devices to search for one digit out of ten whereas, in the binary system, we can represent numbers by a set of mechanical or electrical devices such as a see-saw in the left or right position, a switch in the up or down position, a hole or no hole in a card, a magnetic field in one direction or the reverse direction, a voltage or no voltage. If we consider a lamp, which is an obvious choice after the foregoing examples, then it can represent 1 when on and 0 when off and a row of 5 lamps could represent, in binary form, any number from 0 to 31.

Our next step is to construct a circuit which will add together two binary digits and display the sum and the carry-over digits. Such a device is called a half adder.

Half Adder

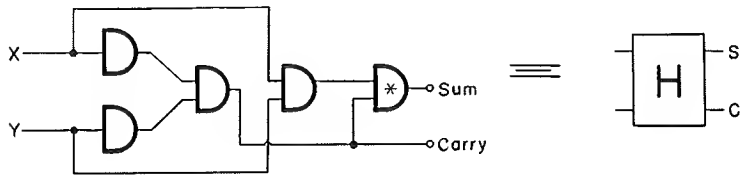
This circuit is required to deal with any one of the following four possibilities:

$0 + 0, 0 + 1, 1 + 0$, or $1 + 1$

The following table lists the possible values of two digits which are called X and Y and indicates the sum and carry we can expect if the addition is carried out.

X	Y	Carry	Sum
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Any network we build should have inputs labelled X and Y and outputs S (Sum) and C (Carry) which obey this truth table. Since the Sum column is equivalent to the 'Exclusive OR' output already described, and the Carry column is equivalent to the AND output, the circuit becomes:



This circuit will fit either the upper or lower part of the NOR board and you can see clearly the AND gate which gives the Carry and the OR gate which is inhibited by the AND gate to give the Sum. Any half adders which are constructed away from the board need only have the sum indicated unless required for demonstration in which case the carry should also be indicated. It will be realised that

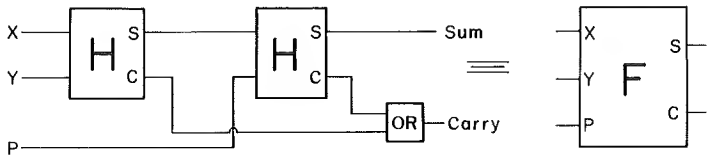
such a unit can be built with five silicon transistors and one germanium indicator transistor plus the other cheap components.

The limitations of the half adder will, by now, be apparent. Only two digits can be added and this is inadequate for most computation. We now look at a more comprehensive unit.

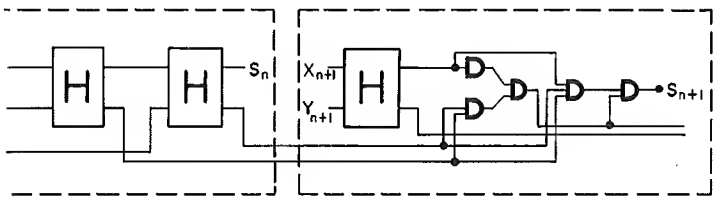
Full Adder

If two binary numbers are to be added, the first digits can be handled by the half adder but subsequent pairs of digits may have to be considered in conjunction with a carry over from a previous addition. Thus a circuit must now be designed to handle three digits, that is, X, Y and a third carry-over digit (P) from a previous addition.

This circuit may be considered as one which adds X and Y by means of a half adder and then that result to P to give the final sum. If a carry results from X and Y, there will certainly be a final carry or, if a carry results from the last addition there will certainly be a final carry over. The full circuit for a full adder is therefore:



Notice here, that we need more than twice the circuitry required for the half adder. This extra OR gate can be dispensed with if a set of full adders are in use and if the adder has its carry over fed into the next adder. The diagram below shows how the separate carry overs from the two half adders are fed to the second half adder in the next unit, each one to two NOR units.



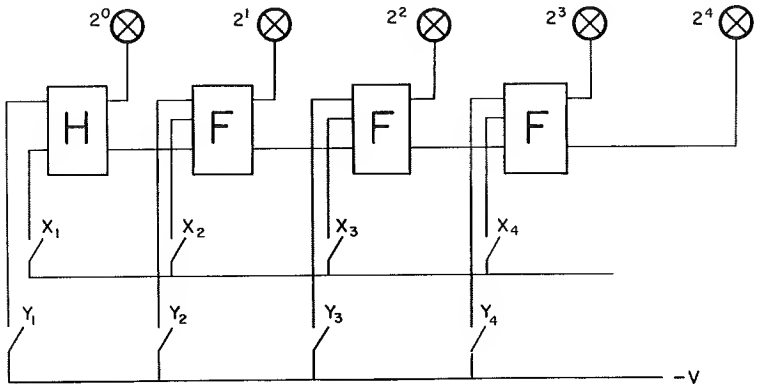
Full adder for nth column of a pair of numbers.

Full adder for $(n + 1)$th column of a pair of numbers.

Full adders are used in all computers and, in many, there are banks of these to enable large binary numbers to be added. As all digits are added simultaneously, this makes the full adder bank a very valuable part of a computer since the time taken to add two twenty-digit numbers is very little longer than two one-digit numbers. Modern computers can carry out an addition operation in less than 0·1 micro-second.

Binary Adder

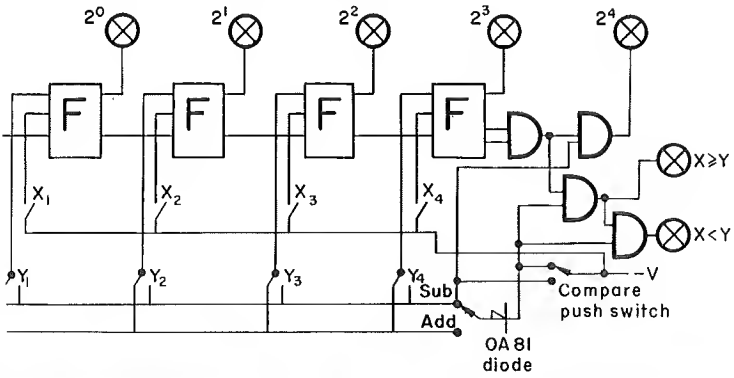
The diagram below shows a set of three full adders and one half adder with indicators (shown away from the units) at each sum output and the final carry output. Remember that the final full adder must have the OR gate for the carry over whereas the other two need not. The arrangement will add any two, four digit binary numbers.

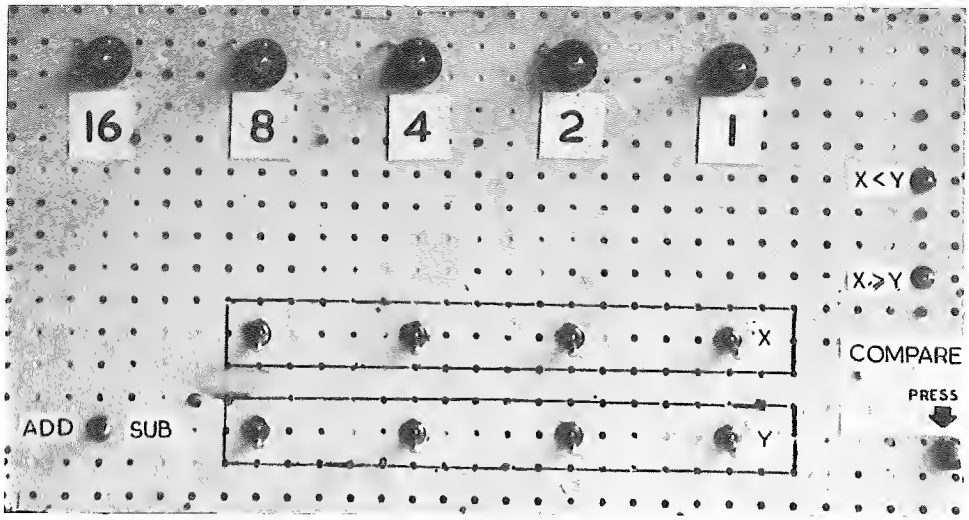


The switches x_1, x_2, x_3 and x_4 will represent the digits of a number, say X and y_1, y_2, y_3 and y_4 will represent the digits of a number Y. The closed position of a switch will represent '1'.

It is usual, when drawing diagrams of binary adders to show the smallest digit on the left which is contrary to the usual way of writing down a number. This is because it is usual for electronic engineers to show flow from left to right and, of course, you will view the circuits this way since they are mounted on the back of the pegboard. Viewed from the front, the number will appear in the usual way with the least significant digit on the right.

It has already been stated in a previous book in the *Contemporary Mathematics Series* that, in fact, a computer can do only three simple things; add, subtract, and compare. Since the above circuit can be developed to subtract and compare we can soon have a model which will carry out the operations of a real computer at comparable speeds. The size of the numbers are not large and our model, at this stage, only carries out operations and does not store the vast quantity of information that a real computer stores.





Model to Add, Subtract and Compare two Binary Numbers.

The circuit on page 57 is an extension of the previous circuit, the following units having been added:

1. A full adder in place of the half adder.
2. Two-pole switches for the digits y_1 to y_4.
3. A two-way switch for switching from add to subtract.
4. A 'Compare' two-way switch.
5. A diode to prevent feed-back.
6. Two NOR units to indicate the relationship between X and Y.

We must first consider how the operations of subtraction and comparison function.

If we desire to subtract the number 1011 from 1101, we can perform the operation by complementing 1011 and adding 1 so that the operation becomes

$$\begin{array}{r} 1101+ \\ 0100 \\ \quad 1 \\ \hline 10010 \\ \hline \end{array}$$

which gives the correct answer provided we ignore the 1 in column five. Our model must allow complementation and also inhibit the fifth column. The diagram (page 57) shows the link between the subtract line and the inhibition point on the OR gate which is part of the last full adder and which is shown separately from the unit for clarity. The diode allows flow to the switch bank y_1 to y_4 which, in the diagram (page 57) is shown to represent the number 1111. When the switch is in the Add position the inhibition is removed and the lamp 2^4 can function.

Note the provision of the first full adder is to enable the addition of 1 to the compliment used in subtraction to be done completely automatically when subtract is selected.

The comparison of two numbers is achieved by making use of the extra 1 which we had to inhibit for subtraction. This extra 1 does not appear if Y is greater than X. Take, as an example, 1001–1110 which would be handled as

$$\begin{array}{r} 1001+ \\ 0001 \\ \quad 1 \\ \hline 01011 \\ \hline \end{array}$$

giving 0 in the fifth column. Thus we can state:
If 1 appears in column five then $X \geqslant Y$.
If 0 appears in column five then $X < Y$.

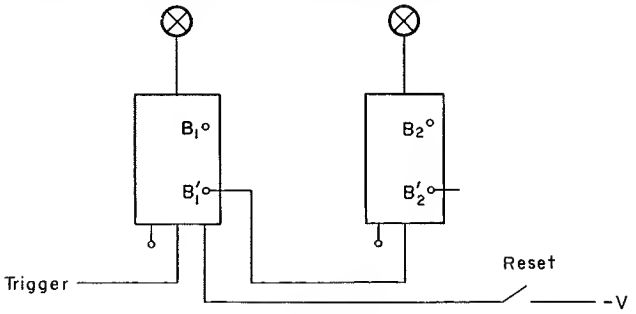
When the compare switch is pressed it feeds the subtract line irrespective of the state of the subtract/add switch and, at the same time, breaks the supply to the add line in case the switch is in that position. The compare switch also inhibits the comparison indicators until depressed when one or other will come on. The diode prevents feed back onto these inhibition points through the subtract switch.

CHAPTER V

The Binary Counter

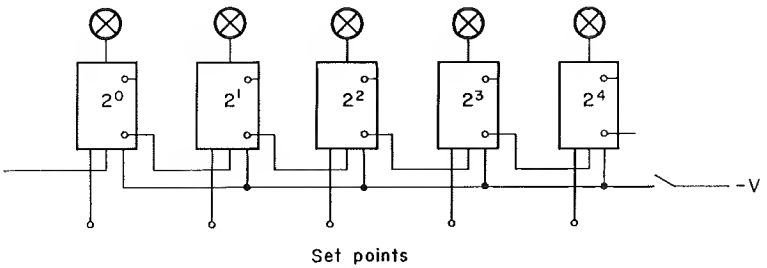
The counter is constructed from a set of Scale of Two units. Referring again to the symbol for the Scale of Two, the lamp in the OFF condition represents '0' and in the ON condition represents '1', the point B is live only when the lamp is ON and the point B′ is live only when the lamp is OFF. A pulse applied at the trigger point will change the state of the lamp, one applied at the set point will leave it in the ON condition while one applied at the reset point will leave it in the OFF condition. The diagram below, shows two units connected so that B_1' (i.e. B′ on unit No. 1) is connected to the trigger point of the second unit. The second unit will change state every time B_1' becomes live which is when the lamp changes from ON to OFF. This gives a simple counting device up to three, or binary 11. The truth table following the diagram below shows the sequence and starts with both lamps OFF after a reset pulse has been applied simultaneously to both reset points. This sequence is repeated every four pulses.

Addition of more units, using the same method of linkage, enables a larger counter to be constructed. Counters with five units enable counting up to 31, which is a very convenient size. If more five stage counters are built they can be arranged in series to count up to higher numbers and can be very useful if high pulse rates need to be measured.



	Lamp 1	Lamp 2	B_1	B_1'	B_2	B_2'
Condition after reset pulse	0	0	0	1	0	1
Condition after 1st trigger pulse	1	0	1	0	0	1
After 2nd pulse	0	1	0	1	1	0
After 3rd pulse	1	1	1	0	1	0
After 4th pulse	0	0	0	1	0	1

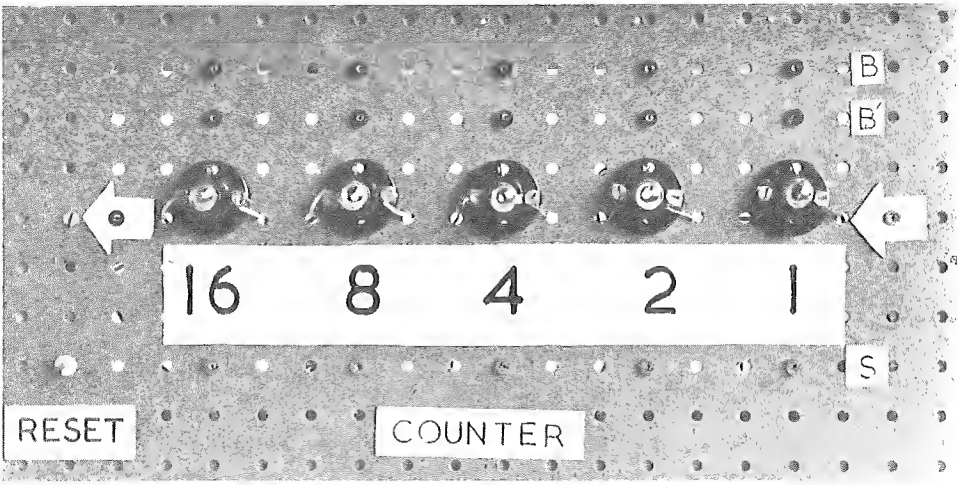
The diagram below shows a complete five stage counter with one reset switch and five set points which enable any number to be entered before the input pulses are applied. To set any particular element a live probe is applied to the desired set point.



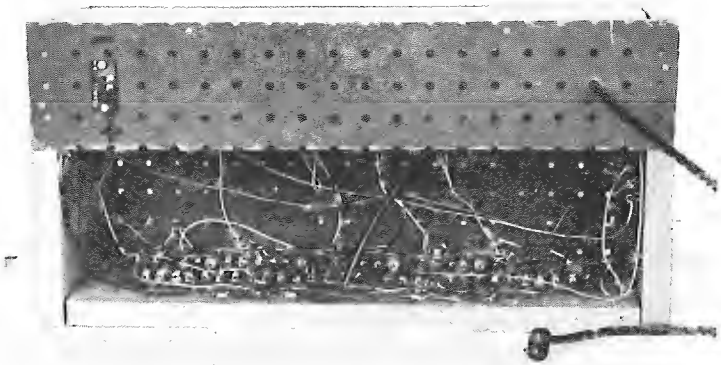
The counter can be constructed on pegboard with each stage mounted on a panel board no larger than $1\frac{1}{2}$ by $2\frac{1}{2}$ inches. The photograph (top of page 62) shows the layout of the front panel of such a counter, the set sockets should be red and the B and B′ sockets black.

At this point it would be interesting to calculate the answers to the following questions and to verify some of the answers by experiment.

1. If the input of the counter accepts pulses at the rate of 1000 per second what period of time elapses before the last lamp lights?



Counter mounted in a free-standing box. The set (S) sockets lie below the lamps and the output (B and B') sockets, above the lamps.



Rear view of the counter box showing the easy access to the circuit and the plug for attaching this unit to a power supply or to a socket on the rear of any other unit.

2. If a second five-stage counter was added to the first, at what rate would the input pulses be entering this unit?

3. If four such counters were arranged in series, how long would it be before the last lamp lights?

4. How many counters do you think would be needed if the last lamp was not to light in an average lifespan of say seventy years.

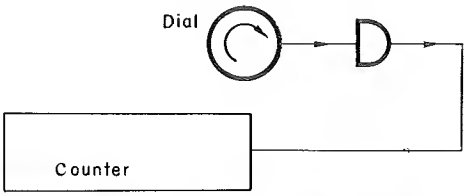
The reader should now devise a simple experiment to find the speed of a pulse clock with a rate of about 1000 pulses per second. Two five stage counters should be used and every effort should be made to minimise the error of the reaction time when using a stop-watch.

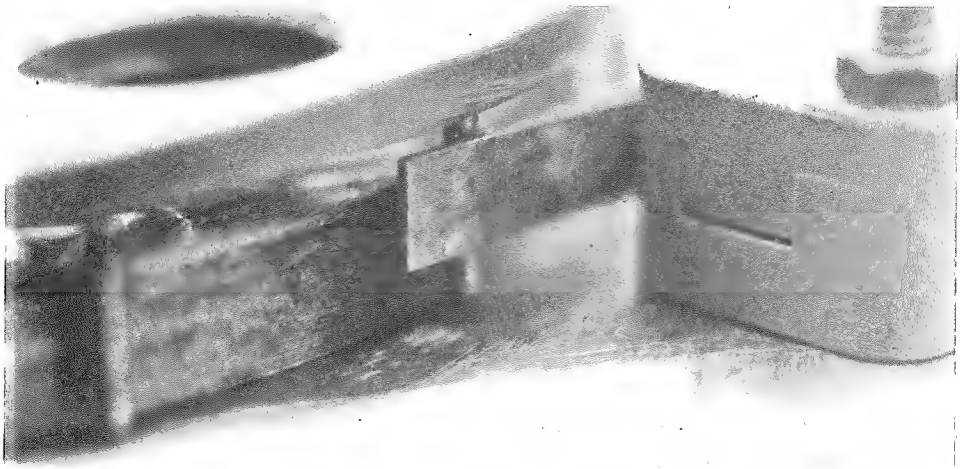
The Operation of the Counter

We are here concerned with the method of feeding the counter. Input can be produced either mechanically or electronically and controlled by either of these methods.

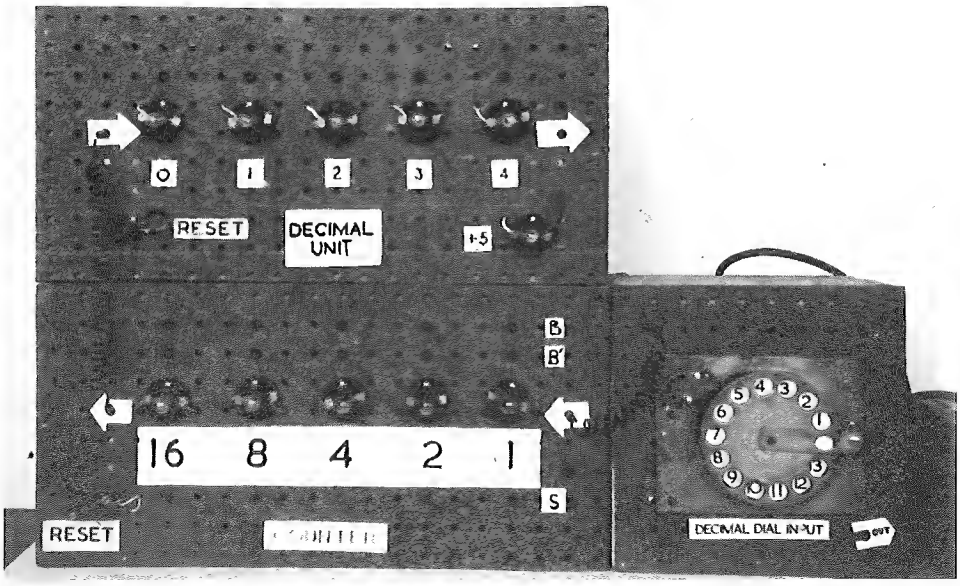
The simplest mechanical method is the single push-button switch with the necessary bounce control unit described in the last chapter. Each press of the button will inject one pulse into the counter.

The G.P.O. type dial also provides a suitable form of input. This also requires the contact bounce control circuit and it will be found that the pulses are supplied during the normal return action of the dial and that the normal condition of the dial is ON. Thus, the number dialled is represented by a number of breaks of this ON condition. For this reason it is necessary to invert the output from the dial by means of a single NOR unit thus:





Close-up of the micro-switch which is actuated by the pins on the perimeter of the dial.



Three units showing how such units can be stacked and interconnected. The dial here feeds the binary counter which carries over into the decimal unit. As arranged, this will count up to 319 in a mixed binary/decimal mode. Output points on either side of the dial enable the dial to be mounted on either side of a unit without the output wire interfering with the dialing operation.

A simple dial assembly can be constructed as shown in the photographs. The dial has short pins entered perpendicular to the dial and on its perimeter. These catch the arm of a micro-switch as the dial is rotated. This unit has the advantage that it works during the activation of the dial and does not need to return to an initial position after use, thereby being much faster than the G.P.O. type. With dial input we have a simple denary to binary convertor and also a simple adder which will add numbers less than ten giving the answer in binary form.

The electronic method of feeding the counter is by far the most important method—the real computer uses this method and, of course, it can be at least one thousand times faster. The demonstra-

tion which follows shows how the flow into the counter can be controlled and how a required number of pulses can be released from the clock by using the counter.

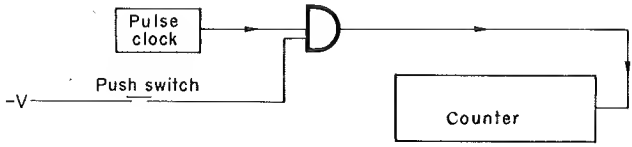
Demonstration No. 1

To show the methods of controlling the pulse flow into the counter and of selecting a given number of pulses.

Apparatus required:

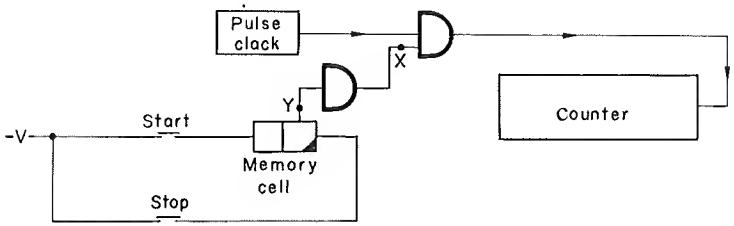
1 Pulse Clock
3 NOR units (one with 5 inputs)
1 Memory Cell
2 Push Switches
1 Counter

Stage I



The diagram shows the layout to enable continuous flow into the counter until the push switch is pressed. This switch can be replaced by a memory cell and NOR unit thus:

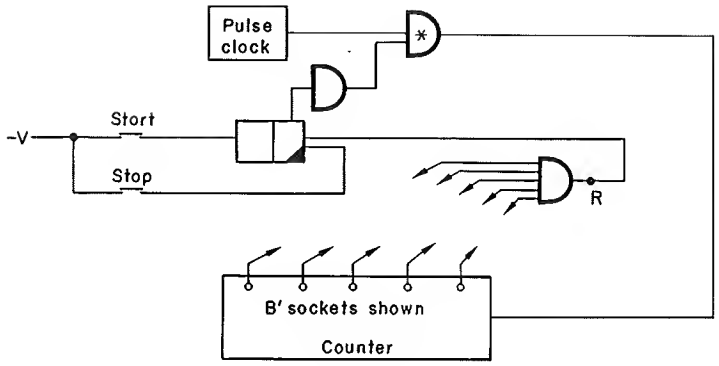
Stage II



The start switch causes the memory cell to switch ON so that Y is alive. X is therefore dead and flow takes place. The stop switch causes the memory cell to switch OFF and so Y becomes dead, X is then live and inhibits the pulse flow. If both switches are pressed then Y is dead and no flow takes place. It is essential that the flow should cease as soon as the stop switch is used even if the start switch is still being held on.

C

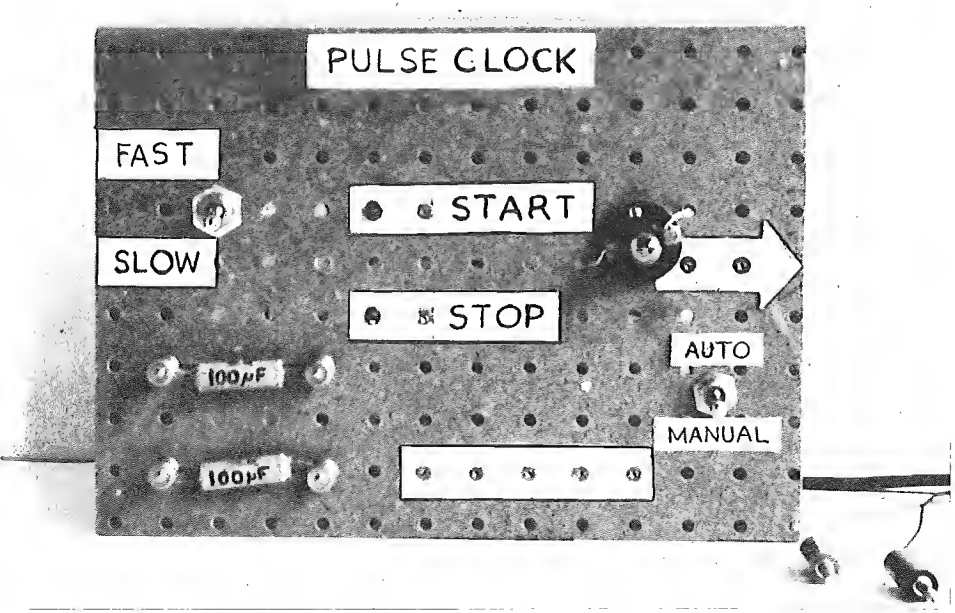
Stage III



This is a development of Stage II in which the memory cell is switched by a signal from the counter. This signal appears at R when no input to the NOR unit is live. The inputs to this unit can be connected to any of the B′ sockets on the counter. Since B′ sockets are dead when the lamps associated with them are ON, the selected sockets will hold R off until the lamps are ON. Thus, if sockets B_4' B_3' and B_1' are connected to the NOR gate, the counter will count from zero to 1101 before all these sockets are dead simultaneously and therefore cause R to be live which switches over the memory cell and inhibits the pulse flow. Since this will happen at any speed, it is suggested that the reader try a fast and a slow speed and so observe the unit in action.

Suggestions for Further Work

1. Since the pulses flowing from the clock can be simultaneously directed to a second counter, see if you can devise a circuit which will add binary numbers and accumulate the result in this second counter.
2. Using a high speed clock and the circuit in Stage I, see if you can simulate the experiment of throwing five coins in which the number of times that 1, 2, 3, 4 and 5 heads appear in throwing 5 coins is recorded and entered on a graph sheet to form a histogram. Remember that the pulse flow is so fast that, when the stop button is pressed, we get a random selection. The ON condition of a lamp can represent a head and the OFF condition a tail.
3. Once the fast rate of the clock has been determined, see if you can devise some simple experiments to find short time intervals such



Pulse Clock mounted in free-standing box, complete with controls. In the AUTO position it is under the control of a counter connected via the row of sockets at the bottom of the box. The capacitors shown can be changed to alter the slow speed.

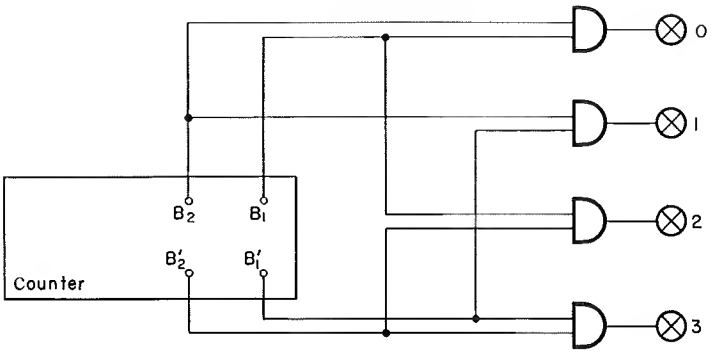
as the time taken for a body to fall 12 inches or to find a person's reaction time. You need something to apply a signal to the start side of the memory cell at the beginning of the period and something to apply a signal to the stop side at the end of the interval. Mechanical switches need not be used—it is possible to introduce photoelectric switching or reed switching.

Demonstration No. 2
Conversion of a Binary Number into the Denary System

Apparatus

Counter with slow pulse clock
4 NOR units each with 2 inputs

This circuit uses the B and B′ sockets of the first two stages of the



five stage counter. We require to convert binary numbers, in this case only up to three, into the denary system. The outputs of four NOR units will be turned on in turn. Cards with the numbers 0 to 3 can be placed beside the lamps of these units. The slow speed clock can be attached to see the sequence in operation or a single push-switch can be used if each stage needs to be examined.

At any instant only one NOR unit has both inputs dead while all the others have at least one live. The full sequence is laid out in the following table:

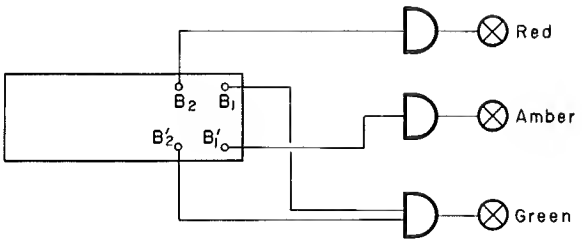
Binary Number	State at NOR inputs	Lamp Conditions	Boolean Expression
00	$B_2=B_1=0$	Lamp 0 on	$(B_2'.B_1')$
01	$B_2=B_1'=0$	Lamp 1 on	$(B_2'.B_1)$
10	$B_2'=B_1=0$	Lamp 2 on	$(B_2.B_1')$
11	$B_2'=B_1'=0$	Lamp 3 on	$(B_2.B_1)$

Sequencial operations are frequently encountered, the most familiar being that of traffic lights in which three lamps, Red, Amber, and Green, are switched on in a special sequence. The next demonstration shows how this can be effected.

Demonstration No. 3
Traffic Light Control

Apparatus

1 Counter with slow Pulse Clock
3 NOR units



This circuit requires less effort than the last one and gives the usual traffic light sequence in which equal lengths of time are given to each part of the sequence. It is possible to vary the time of different parts of the sequence by using more stages of the counter. The table below shows the complete sequence:

Binary Number	RED	AMBER	GREEN
00	ON	OFF	OFF
01	ON	ON	OFF
10	OFF	OFF	ON
11	OFF	ON	OFF

See if you can now design a circuit which will allow the Red and the Green to be on for three times longer than Red and Amber or Amber alone.

Given equal lengths of time for each part of the sequence the probability that any particular lamp will be on if a random stop is carried out is:

Probability of Green $= \frac{1}{4}$ P(Amber) $= \frac{1}{2}$
P(Red) $= \frac{1}{2}$ P(Amber *and* Red) $= \frac{1}{4}$ P(Amber *or* Red) $= \frac{3}{4}$

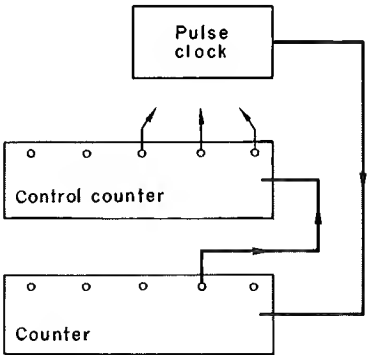
Try a number of random stops using a high speed counter and see if these probabilities work in practice.

Demonstration No. 4
Multiplication and Division by numbers which are powers of two

Apparatus

2 Counters
1 Pulse Clock

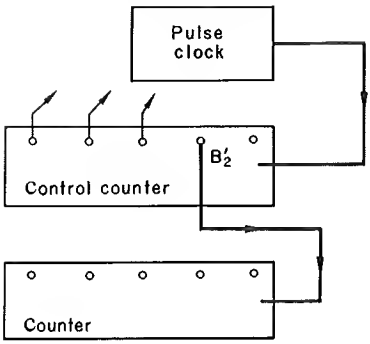
Multiplication



The arrangement here is to choose every 2^nth pulse flowing into the lower counter and allow the control counter to count these and switch off after the required number has been chosen. For example, if we wish to multiply 7 by 4 the circuit above shows that 7 is selected on the control counter and the output of the second stage of the lower counter, B½ is connected to the input of the control counter. The B½ socket changes from dead to live on every 4th pulse from the clock. When the control counter registers 7 the clock is switched off and the lower counter will contain the answer 28. Notice that the labels 1 to 16 on these counters show clearly the 7 and 28 but not the 4. This 4 (the multiplier) can be indicated by placing cards labelled 2, 4, 8, 16 next to the B′ sockets on the lower counter. This demonstration is limited to problems in which the answer is less than 32 but can be extended if a third counter is available.

Division

This is a simple variation on the last arrangement. The answer again appears on the lower counter while the dividend is selected on the control counter. The diagram on page 71 shows the method of dealing with 28 ÷ 4 in which the control counter (opposite) counts up



to 28 with every 4th pulse being recorded on the lower counter. Extensions are again possible by adding a third counter to the upper register so that the dividend may be increased in size. If this is done, care must be taken to see that the control circuit is not overloaded—a dividend containing more than five binary '1' digits should not be taken.

We have seen a number of operations performed by the counter and, in particular, we have seen the counting operation itself which is really a process which selects all the different arrangements of the on-off states of 5 lamps. This can now be used to solve certain logical problems by allowing the counter to select all the possibilities and to react to the sets which offer a solution to the problem. We shall now consider two such problems.

Problem No. 1

Consider the three subjects, Maths, English, and Latin. A student taking a certain course must obey the following conditions:

1. English must be taken.
2. Maths or Latin must be taken.
3. English and Maths cannot be taken together.

Which of these three subjects can be studied together?

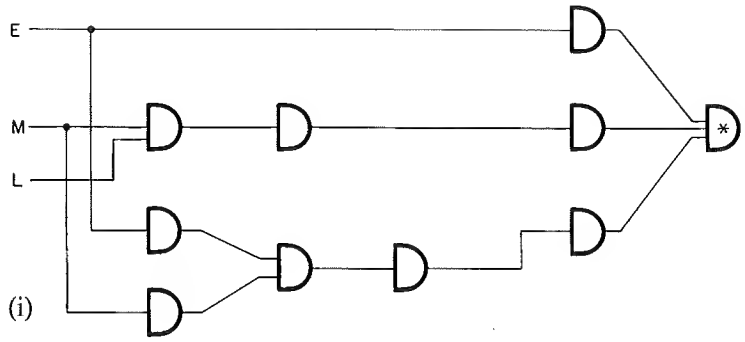
The stages in the solution of this problem are listed below:

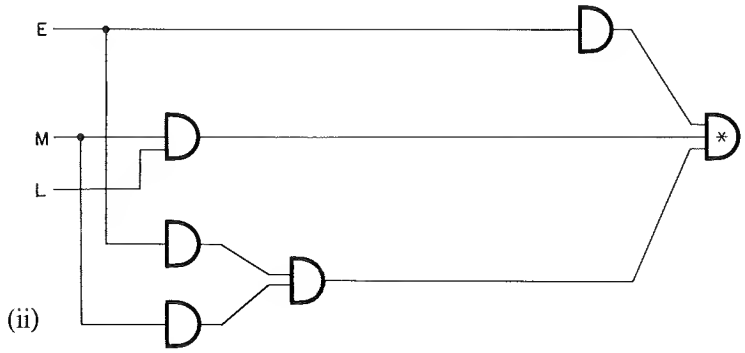
Stage I

Build up the NOR logic circuit diagram in a similar way to that used in earlier examples. *See over* (*i*).

Stage II

Simplify this circuit if possible and arrange it on the NOR logic board. *See over* (*ii*).

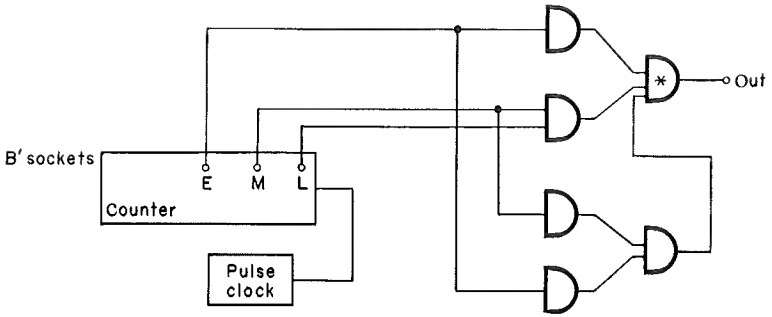




Stage III

It is now necessary to go systematically through all the possibilities of selecting, or rejecting, the three subjects. The counter is used to do this automatically by feeding the B sockets of the first three stages to the points marked L, M, and E, on the logic board. The first three stages should be labelled L, M, and E, and the lamps for stages four and five removed to avoid confusion.

The diagram on page 73 shows the complete layout while the truth table shows the selections which will be generated by the counter and indicates which conditions are satisfied and also the one selection which obeys all conditions simultaneously. This table is presented to help in the understanding of the problem and is not essential to its solution.



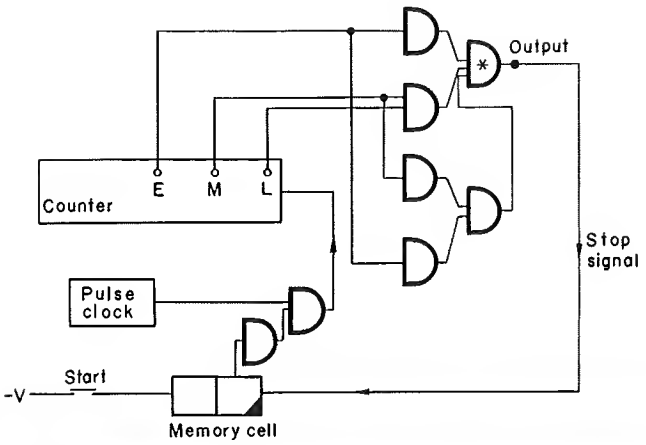
M	E	L	E must	M or L	(E & M)'	OUT
0	0	0	0	0	1	0
0	0	1	0	1	1	0
0	1	0	1	0	1	0
0	1	1	1	1	1	1
1	0	0	0	1	1	0
1	0	1	0	1	1	0
1	1	0	1	1	0	0
1	1	1	1	1	0	0

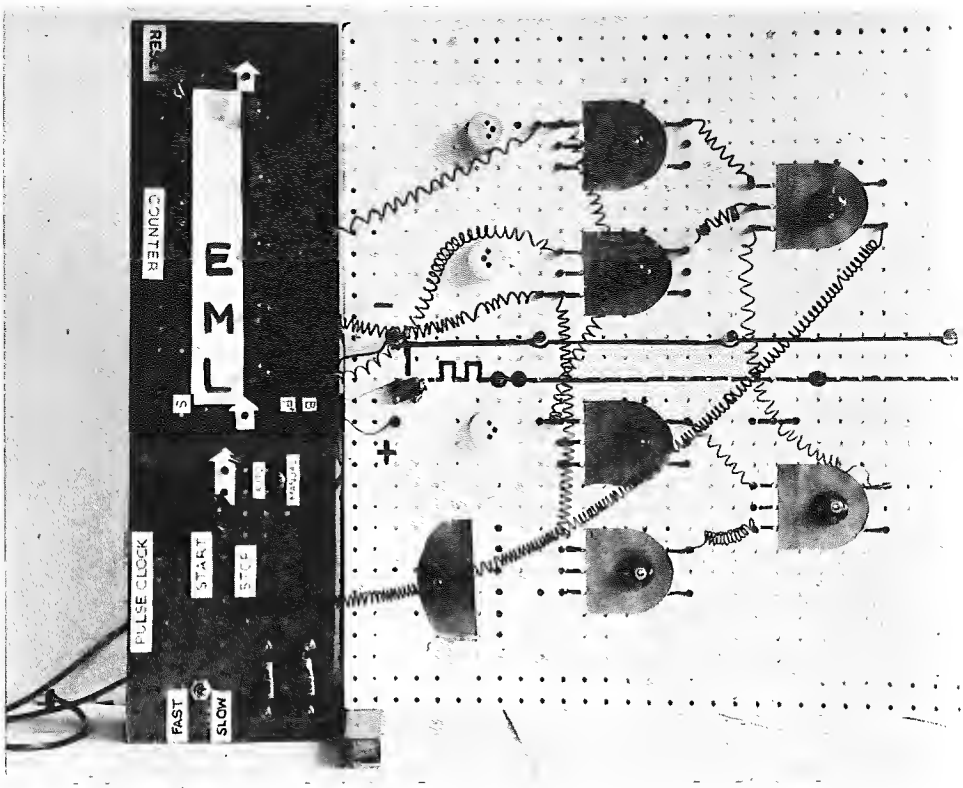
A slow pulse rate, of about 2 seconds per pulse, should be chosen so that all 8 possibilities will take 16 seconds. Only when the correct combination is selected will the output lamp switch on. The solution is indicated on the counter by the lamps in the on condition above the appropriate label.

The above circuit will allow the cycle of operations to continue indefinitely and shows the solution for only 2 seconds. The addition of a few control elements will allow us to stop automatically when a solution has been found. To do this the output is fed to a memory cell controlling the pulse flow. The complete circuit is shown on page 74.

Problem No. 2

The last problem shows how a number of conditions, applied simultaneously, restrict the selection that can be taken. Naturally, the problem is so simple that we can see the correct solution without all this circuitry. However, large problems can be handled if sufficient





Counter, Pulse Clock and Logic Board arranged to solve the English, Maths, Latin problem.

NOR units are available. The possibilities can be generated by the counter which will stop when a satisfactory combination is selected. Let us now consider a problem in which there are 5 variables and which lays down more conditions. The conditions will be taken in turn and a suitable logic circuit constructed for each one.

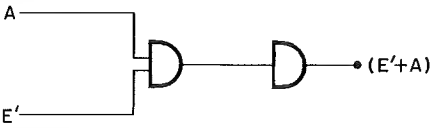
I would like to take some friends to the theatre, there are 5 of them but there are certain restrictions on whom I should take:

1. Eric will only go if Alice is there.
2. Brenda won't go with David unless Eric is there.
3. Connie won't go with David or Alice.
4. Alice won't go if the boys are together.

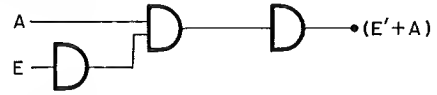
What must I do?

There are many solutions to this problem—10 including the case where no one is taken. Each restriction will be taken in turn and we will write down (*a*) the logical expression, (*b*) the Boolean expression, (*c*) the NOR logic circuit.

1. Eric will only go if Alice is there.
   (*a*) The presence of E implies the presence of A
   i.e. $E \Rightarrow A$.
   (*b*) The Boolean expression E′ or A i.e. $E' + A$.
   (*c*) The NOR circuit which is an OR gate into which is fed E′ and A thus:

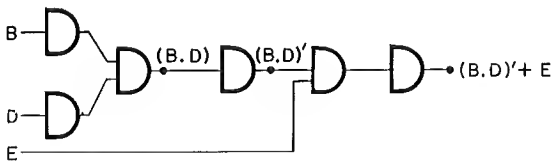


or, more conveniently,



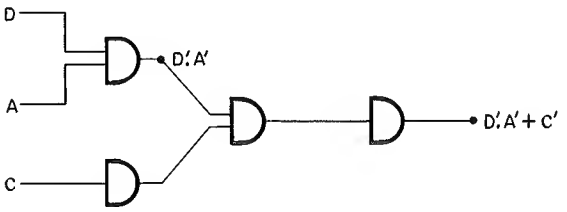
2. Brenda won't go with David unless Eric is there too.
   (*a*) The presence of both B and D implies the presence of E
   i.e. $(B \wedge D) \Rightarrow E$.
   (*b*) The Boolean expression $(B.D)' + E$.

(*c*)



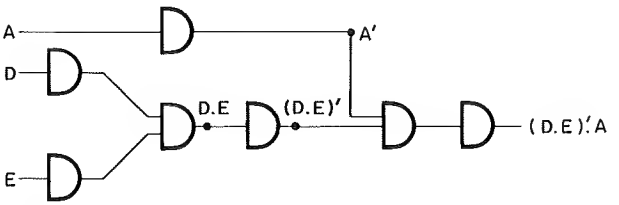
3. Connie won't go with David or Alice.
   (*a*) The presence of D or A implies the absence of C
   i.e. $D \vee A \Rightarrow C'$.
   (*b*) $(D + A)' + C'$ which can be written as $D'.A' + C'$ (D'Morgan's Laws).

(*c*)

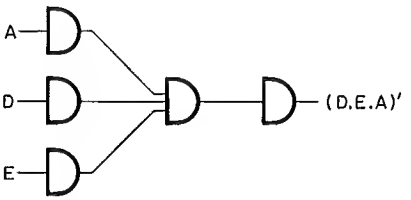


4. Alice won't go if the boys are together.
   (*a*) The presence of D and E implies the absence of A
   i.e. $D \wedge E \Rightarrow A'$.
   (*b*) $(D.E)' + A' = ((D.E).A)'$ (D'Morgan's Laws).

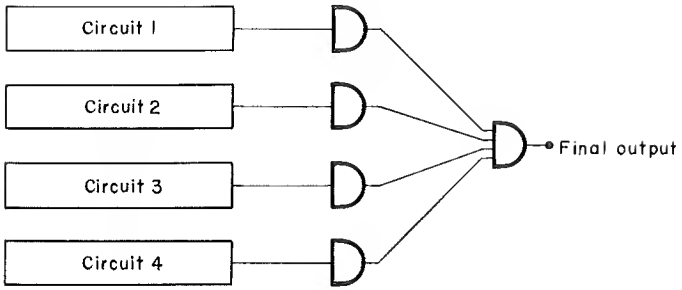
(*c*)



which simplifies to



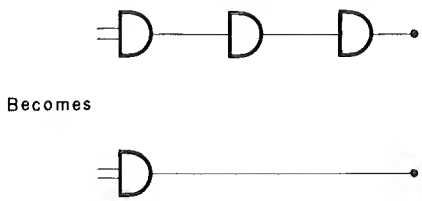
The output point on each of these four circuits is only alive if the quoted restriction is not violated. Since each of these four points must be alive simultaneously for all the restrictions to be obeyed we can feed each output to an AND gate, the final output point will only be alive if all the four outputs are alive.



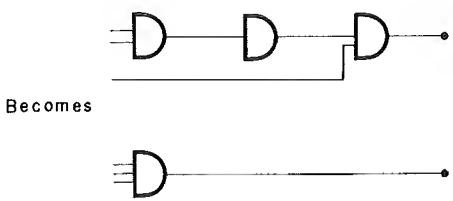
This complete circuit can now be simplified in certain ways:

(i) Some NOR units can be used in more than one circuit.

(ii) Two NOR units in series can be removed thus



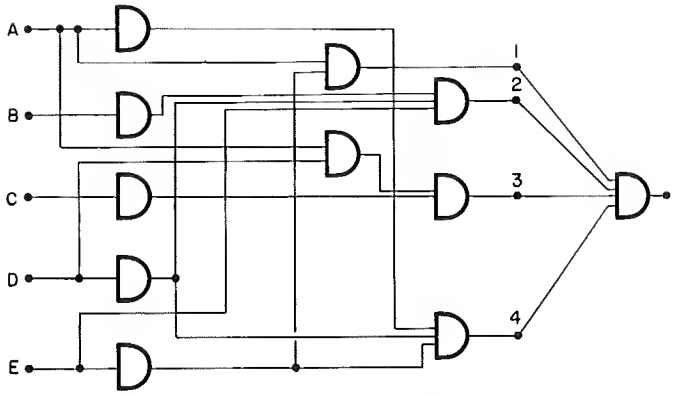
(iii) Since $(A + B)'.C' = A'.B'.C'$



The whole of this circuit can be arranged on the NOR logic board which contains 10 NOR elements and one OR gate but we have added one more NOR element with 6 inputs which can be used in the final stage of a six statement problem (only four are used in this problem).

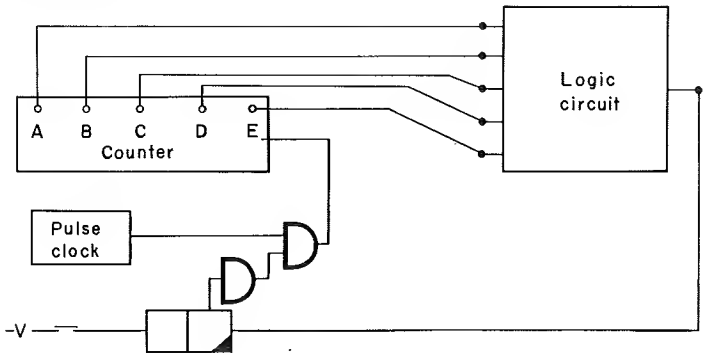
The complete circuit in its simplified form is shown on page 78 (top).

Once this has been arranged on the logic board, the whole problem can be analysed using manual input and observing the input states, the states at points 1, 2, 3, 4 and the state at the end point. Because of the economy in NOR units the state at 1, 2, 3 and 4 must be '0' for the final unit to be in the '1' state.



It is now possible to read out solutions automatically to this problem by feeding the points A, B, C, D and E from the B points of the counter with the lamps 1 to 5 labelled A to E.

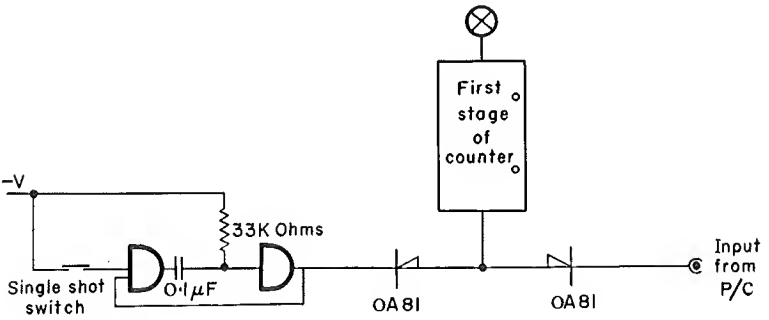
The complete circuit for automatic generation of solutions can now be given:



Operation

Press the start switch. The counter will count until a correct combination appears, at which point the memory cell will be reset by the output from the logic board. The lamps above certain of the A to E labels will be ON. These indicate a solution but not necessarily the only one. It is necessary to restart generation of solutions but the memory cell is held off by the output from the logic board. This is achieved by changing the state of the first stage of the counter which will then read the next combination to be tested. This is effected by applying a single pulse to the first stage by means of a

press switch via a time delay circuit. Diodes, from both inputs to this stage, are necessary to prevent feed-back.



Exercise 3

1. Design a circuit for conversion of binary numbers into the denary system up to binary 111, denary 7.

2. Design a circuit to operate a set of traffic lights so that the time periods of the RED, AMBER and RED, GREEN and AMBER are in the ratio 6 : 1 : 8 : 1.

3. If you had a pulse clock giving 1 pulse per second and you required a device to be switched on for a period of time of t seconds and off for a period of $32 - t$ seconds every 32 seconds, where $t < 32$, show how you would design such a circuit for the following cases:

(i) where $t = 16$ seconds,
(ii) where $t = 4$ seconds,
(iii) where $t = 5$ seconds.

4. A man and his wife walked into a car showroom to be greeted by the salesman with the statement 'Any of our models can be supplied with Automatic Transmission, Power Brakes, Safety Belts, Transistorised Radio, or Reclining Seats'. The man stated 'If I have Automatic Transmission then I must have Safety Belts and Power Brakes'. His wife then stated 'If you have Power Brakes fitted then I must have a Transistorised Radio and Reclining Seats'. The man

retorted with 'If I have Power Brakes and Radio then I can't afford to have Automatic Transmission'. Design a logic circuit which will indicate which of these extras can be fitted to the car to satisfy all these conditions.

5. I am prepared to study any of the subjects, Art, Biology, Chemistry, English or French. The following rules apply however:

(i) If Biology is taken then Chemistry must also be taken.
(ii) If Biology and Chemistry are taken then Art and French cannot be taken.
(iii) If English is not taken then Biology or Art must be taken.
(iv) If French is taken then English and Art or English and Biology must be taken.

Design a logic circuit which could be used to select suitable subject combinations.

6. Three television cameras are mounted inside a special research laboratory where experiments involving radioactive materials are being carried out and where it would be unsafe for humans to be present. The cameras, A, B, C are connected to a single screen so that only the picture received by one camera can be viewed at any one time. The activity viewed by A is more important than that viewed by B or C. The sequence follows the following pattern: 7 intervals of time are spent on A followed by 1 on B, then 7 more on A and then 1 on C. This sequence is repeated continuously. Design a circuit for controlling this sequence, given a 5 stage counter, a pulse clock capable of a speed of one pulse per 5 seconds and the knowledge that B and C must be on for 10 seconds each.

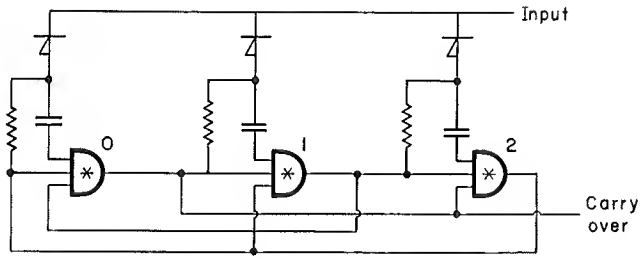
7. When leaving a submarine, three hatches H_1, H_2, H_3 must be opened, in order, by an automatic device, the correct sequence being obviously essential. Design a logic network to send signals to three motors M_1, M_2, M_3 which will open the doors at intervals of 10 seconds and then switch off after the operation is complete.

Counters other than Binary

Counters other than binary counters can be constructed in other ways than routing information from a binary counter. The first of these, known as a ring of three, can be assembled on the NOR board and, as its name implies, counts in the scale of three. The second one, a decimal counter, is too complex to assemble on the board and the photograph will show a counter of this type mounted into one of the usual boxes.

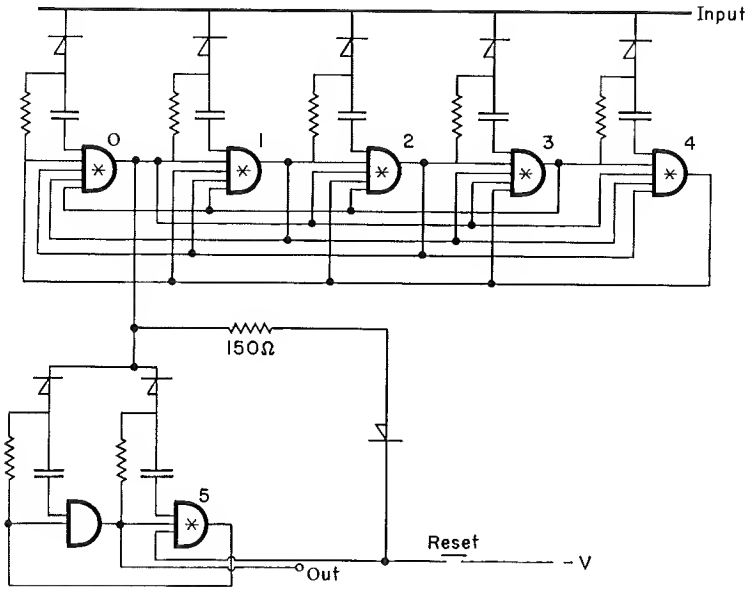
Ring of Three

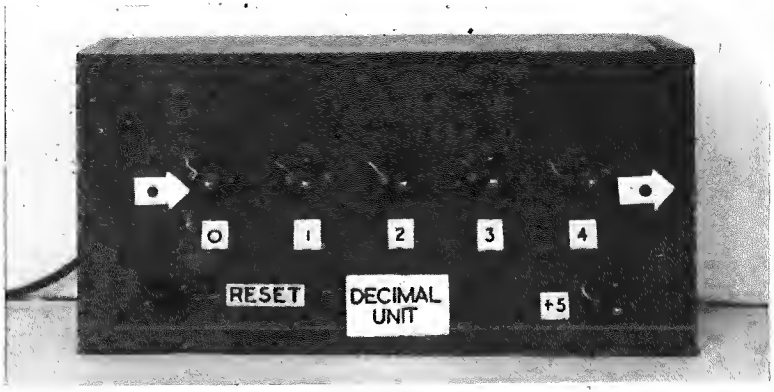
This is a simple extension of the Scale of Two circuit in which three NOR units are used in place of two with the routing network increased to cover the extra unit and with every NOR output connected to the input of each of the others.



Sets of these rings of three circuits would be used for counting in a number system based on three, for example, two rings of three could be used to count feet up to two yards, two feet. The output of the first unit will give the carry over to the next ring of three.

A Decimal Counter





Decimal Counter

Although this unit is not incorporated into the model computer it is of interest in itself and can certainly be used in conjunction with the other basic units to show conversion from binary to decimal and from decimal to binary systems.

The complete unit shows a ring of five NOR units working in conjunction with a scale of two which extends the range to 10. Lamps labelled 0 to 4 cater for the numbers 0 to 4 directly and, in conjunction with a lamp labelled 5, from 5 to 9. Thus 7 is registered as 5 + 2 while 2 is simply shown as 2.

The ring of five is an extension of the ring of three in which the output of each NOR unit is fed to the input of each of the other four and the carry over is taken from the first unit (i.e. the one which will be labelled '0'). Resetting the unit is effected by applying pulses simultaneously to the normal reset on the scale of two and to the output point of the first NOR unit on the ring of five. The circuit for this reset is slightly different to all the others and should be specially noted. The resistor in the circuit allows the correct potential to be applied at the reset point.

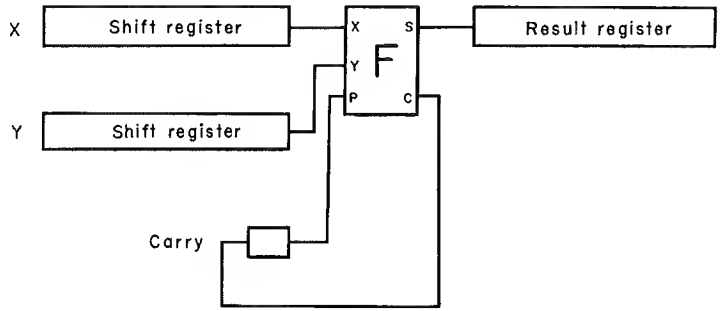
CHAPTER VI

The Shift Register

The shift register is a unit in which the binary number can be shifted to the right to form a new binary number, the digits of which are in the same relative position. The set of binary numbers below show the effect of shifting—each shift has the effect of dividing by two.

1101000	104
110100	52
11010	26
1101	13

In some small computers the digits from two binary numbers can be moved into the end position in turn and a single full adder can then perform an operation on the pairs of digits as they leave the registers. The shift register to be described is capable of storing a number with 10 binary digits (bits) which is equivalent to a decimal number of 1023. The cells containing the digits must be capable of transferring their contents to a neighbouring cell and accepting information from the other neighbouring cell. The diagram below shows the way in which 3 registers can be used with a full adder and a store for the carry-over digit.



The time necessary to perform one addition operation is N x t where N is the number of cells in the shift register and t is the time

for one shift. In our example N would be ten and t for the model to be described later is about 0·002 seconds. Thus, a time of about 0·02 seconds is used in performing one complete addition operation. A set of costly full adders would perform this whole operation in one pulse length. The serial method (i.e. operating on one pair of digits at a time, using shift registers) is better than the parallel method (using full adders) for the educational display model as it shows more clearly, and more slowly if desired, the operations of the parts which make up a computer.

Let us consider the bistable (memory cell) and see how it can be used as an element in the shift register. The diagram below shows a group of 5 such cells each carrying a piece of information as shown.

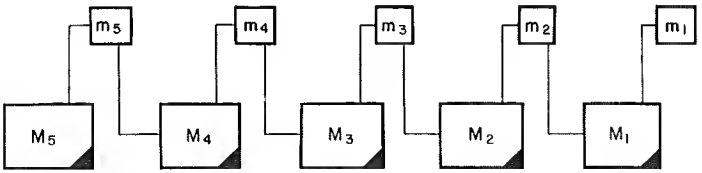
0	1	1	0	0
Cell No. 5	4	3	2	1

If one shift to the right is required then the following table indicates the operation we need to perform on each of the 5 cells.

No. 1 Rejects 0	Accepts 0 from No. 2
No. 2 Passes 0 to No. 1	Accepts 1 from No. 3
No. 3 Passes 1 to No. 2	Accepts 1 from No. 4
No. 4 Passes 1 to No. 3	Accepts 0 from No. 5
No. 5 Passes 0 to No. 4	Read 0

Note that a cell such as No. 4 passes and accepts unlike information. We must see that the information (1) passes out before the new information (0) enters the cell. Clearly one cell must have already passed on its information before it accepts that from the previous cell. To do this reliably a method using an intermediate memory cell has been adopted. There are other faster circuits but this one is easy to construct, is based on the preceeding circuits and is not so critical as the others. Also the whole shifting operation can be more easily checked with a simple voltmeter.

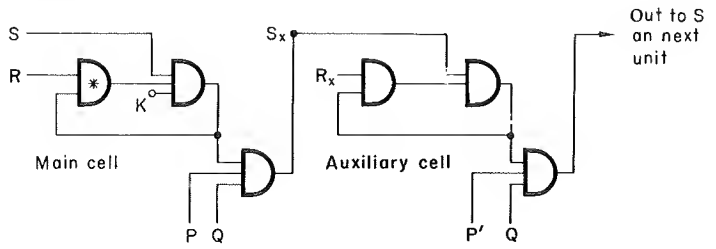
An Electronic Shift Register



The shift register is made up of 10 stages. Each stage of the shift register contains two memory cells, one main cell which has the lamp indicator, and an auxiliary cell without indicator. The diagram opposite shows only five stages, the main cells M_i ($i = 1$ to 5) with the auxiliary cells (m_i for stage i). The procedure for one shift is as follows:

Step 1 Information in cell M_i is transferred to empty cell m_i.
Step 2 Cell M_i and all other M cells in the register are reset to 0.
Step 3 Information in cell m_i is transferred to empty cell M_{i-1}.
Step 4 All m_i cells are reset to 0.

Thus a complete shift needs 4 steps—this is a disadvantage since it reduces speeds to 25% of what could be expected but this is still fast enough for an educational demonstration machine. The transfer from M to m cells and from m to M cells require NOR gates which release information at the correct time. The diagram below shows one complete shift element and we will trace through the steps on this diagram.



The main memory cell is made up of the first two NOR units one of which has a lamp indicator. This lamp is ON if the cell is said to contain 1 and it can be reset by a pulse applied to R and set by a pulse applied to S or to the socket K. When the lamp is ON the link to the third NOR unit is dead. When the lamp is off the link to the third NOR unit is alive.

The auxiliary cell is virtually the same, apart from the lamp indicator. Now let us go through the four steps.

Step 1 Information (1 or 0) in the main memory cell has to be transferred to the auxiliary cell via the third NOR unit in the diagram. This is done by causing points P and Q to be both dead—throughout the rest of the cycle one, or both, will be live. The condition at S_x will now depend on the link with the main cell. If 1 is contained in the cell the link to the third NOR element will be dead so that the output of this element is live hence S_x will represent 1 and so set the empty auxiliary cell. If 0 is contained in the main memory cell the link will

be live and so the output of the third NOR element will represent 0 so that the auxiliary cell will remain empty.

Step 2 Normal supplies are returned to P and Q and a pulse applied to R to reset the main cell.

Step 3 The information in the auxiliary cell is transferred to the main cell in the next shift element by causing P′ and Q to be both dead. The output to the next unit will match the contents of the auxiliary cell, and so transfer its contents to the next main cell.

Step 4 Normal supplies are returned to P′ and Q and a pulse applied to R_x to reset the auxiliary cell.

Thus the cycle of 4 steps has been completed. This cycle is to be carried out on all shift elements of the shift register at the same time so that the points R, R_x, P, P′, Q, must have the necessary states at the right times.

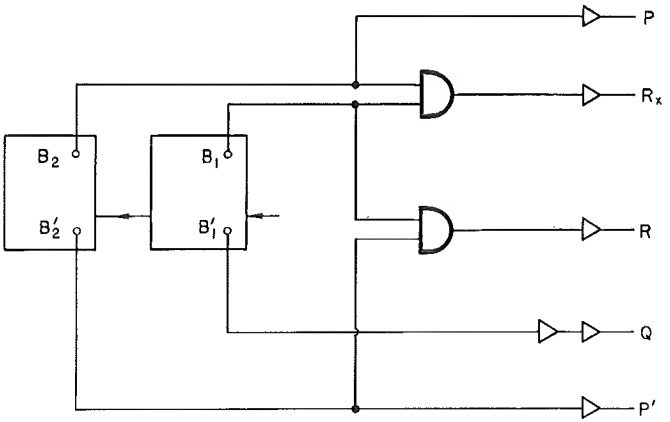
This may be represented in a table, thus:

Stage	Stages at				
	R	R_x	P	Q	P′
1	0	0	0	0	1
2	1	0	one or other or both 1		0
3	0	0			0
4	0	1			1

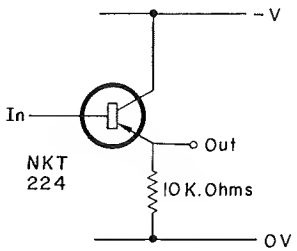
Each element of this shift register needs 6 NOR elements, one of these with an indicator lamp. Three inputs are needed to 3 of these units and two inputs to the remaining 3 units. This does mean rather a lot of components which need to be contained in a small space. It is possible to mount these on a board 1·5 in. × 4·3 in. with 9 tags on each side in which one end of the resistors associated with R, R_x, P, P′ and Q, are not given a tag. These resistors stand perpendicularly to the panel board and connecting wires run along the entire register to connect all the R points together, all the R_x points together, etc. When this register is working, the lamps indicating any number will be alight for 3 stages and off for 1 stage during the 4 stages of the shifting operation.

In order that the points R, P, Q etc. should have the required states at the right time a special counter with a routing device is

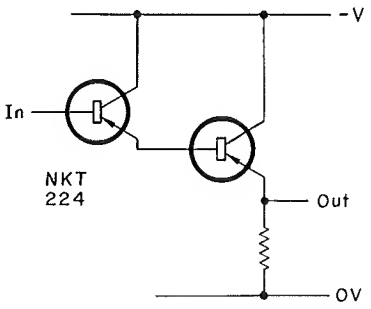
needed. This presents a problem very much like the traffic lights problem since we again want a sequence of 4 operations. The diagram below shows such a unit with the end points marked with the letters showing the points to which they will be connected on the shift register. Since each of these end points will have to feed so many points on the shift register (at least ten) amplifiers are needed to cope with these extra commitments.



The amplifiers in the above figure are emitter follower amplifiers and are constructed very simply and cheaply with one NKT224 transistor.



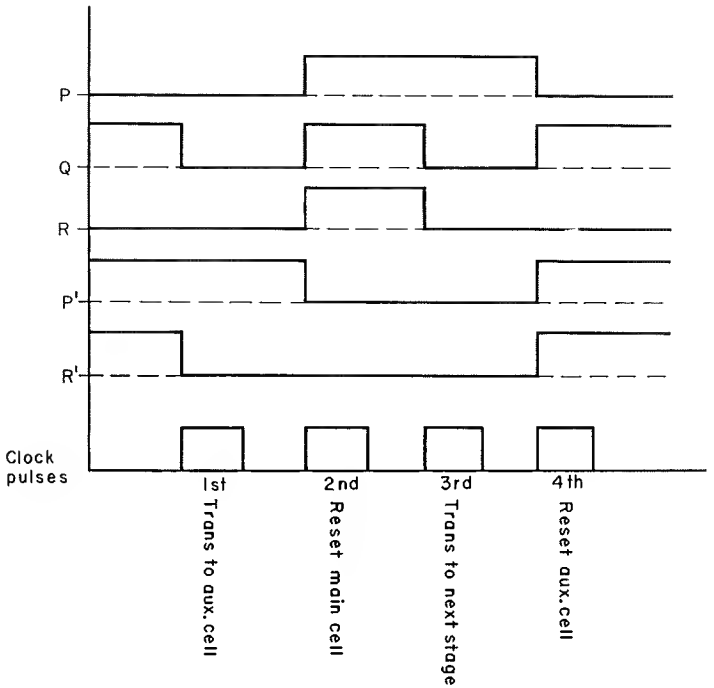
However, since the Q line feeds twice the number of points and a single emitter follower amplifier would be overloaded it is necessary to install two, thus:



The states at the points indicated in the selector diagram can be shown in the following table and pulse diagram

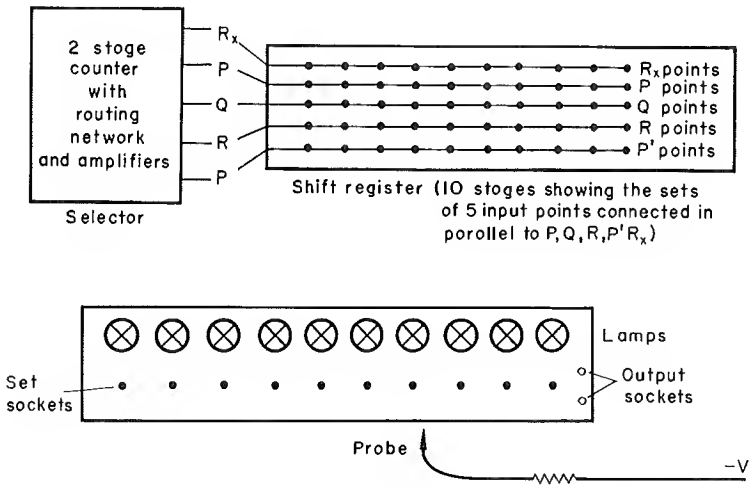
B'_2	B_1'	B_2	B_1	P	Q	R	P′	R_x	
1	0	0	1	0	0	0	1	0	Step 1
0	1	1	0	1	1	1	0	0	Step 2
0	0	1	1	1	0	0	0	0	Step 3
1	1	0	0	0	1	0	1	1	Step 4

The standing position (Binary counter at 00) is in the step 4 position so that steps 1, 2 and 3 correspond to binary 01, 10 and 11.

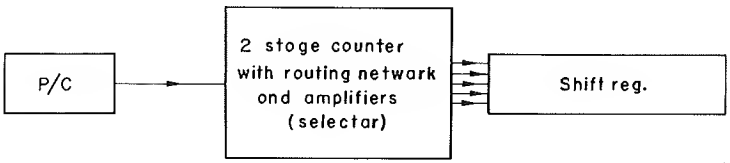


The complete set of 10 stages of the shift register can be mounted on peg board 24 in. by 7 in. with the circuit on the back of the board

and the lamp and set socket on the front. It is this set socket which needs to be touched with a live probe if a binary '1' is to be entered into the register.



Operation of the Shift Register

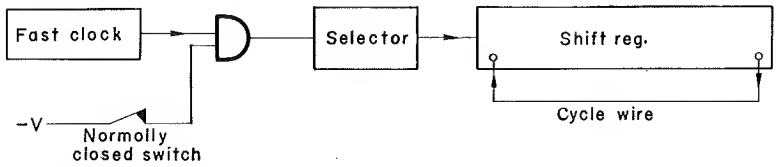


Arrange the clock, selector and shift register as in the diagram.

If any lamps are alight then a live probe touched onto the R and R_x leads will reset them and it is as well to reset the 2 stage counter by the usual method. There is no need for a special reset of this counter as the completed computer switches itself off in the required position (see later)—however, at this stage we may not be in the zero state and it is as well to start in this state. Set a 1 digit in the extreme left element of the register by touching the end set point with the probe. Now start the pulse flow at a slow rate (try about $\frac{1}{2}$ sec. pulses) and watch the digit move slowly along the register. If the pulse clock has $\frac{1}{2}$ sec. pulses then the lamp will remain on for $1\frac{1}{2}$ sec., then off for $\frac{1}{2}$ second before the next lamp alights. After 20 seconds the register will

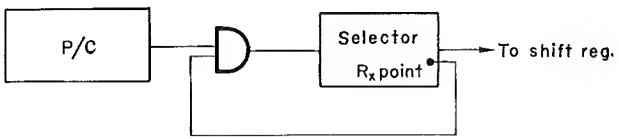
appear empty, the digit will apparently have moved along and been pushed off the right-hand end of the register. If the output point of the last stage is connected to the input stage of the register (i.e. the red, set socket of the first stage), the digit will appear to cycle round to the left-hand side of the register. It will return to its initial position after 10 moves, or after 40 pulses have been released from the pulse clock. Stop the pulse flow and set up another number with more than one digit and watch it cycle round. Now remove the cycle wire from the left hand socket and attach it to the next input socket. Any number now entered on the register will cycle once round in 9 moves or after 36 pulses have been released from the clock. Try a number of different positions for the cycle wire with different binary numbers and observe their movement.

Insert the cycle wire and have a push switch control linked to a high speed pulse clock.



Reset the shift register and enter a single digit anywhere on the board. Push the press switch—the digit will now cycle round the board at high speed—it is not difficult to have the 2000 p/sec. speed on the clock giving 50 complete cycles/second of the shift register. Now release the button. This stops the cycle operation but the 2 stage selector may be in any of the stages we have already discussed—in one of these stages, the digit is contained in the auxiliary cell with the main cell empty so that the digit would not appear on the register if this particular point had been reached. If, however, any of the other 3 stages had been achieved, one lamp would be alight. Thus, in a random stop, the chance of an empty register is 1 in 4.

Try a few runs and see if this works in practice. If we want to be certain that the operation ceases in the correct position, the switch control link should be attached to the R_x line so that the pulse flow only stops when this is live which is, of course, the correct point in the cycle.



Now that there will certainly be a number visible in the register when we press the button we can proceed with some more interesting experiments.

Use of the Shift Register in Statistical Work

Arrange the register to cycle round 10 stages, and enter 1 digit at any point. Remember that 10 shifts are necessary to move it round to its original position, 40 pulses are emitted from the clock in order to do this and this can happen in about 0·02 seconds. Now press the button to allow the operation to commence—you will be unlikely to see the movement of the digit since any one of the lamps will be on for only about 0·0015 seconds during each 0·02 seconds. When the switch is released the shifting operation will cease as soon as the next pulse arrives on the R_x line. There is obviously only a one in ten chance that the digit has arrived back at its original position or even to any other position in the register which you may have in mind. If you now view only the end lamp and consider the probability that it will be on when the button is released, it is also 1/10. If 2 digits are entered and cycled round, the probability of the end lamp being alight at a random stop, is 2/10—for 3 digits it is 3/10 and so on. Since you can cycle with this register through any number of stages from 3 to 10 you can arrange experiments involving probability in the range x/y where

$$10 \geqslant y > x > 1 \text{ and x and y are integers.}$$

This is, in effect, a variable electronic die and one that is not loaded. This means that you have the means of carrying out experiments on chance. Here, for instance, is an interesting little problem which can be worked by the binomial distribution or could be examined experimentally on this register.

Example 1

It is found that the probability of there being a faulty component, of any kind, in my new car during the first month is 2/7. If my 4 friends and I buy new cars on the same day, what is the probability that 3, and only 3, of us will have trouble during the first month?

Solution

Let the probability of failure be p (i.e. $p = 2/7$).

Then, if q is the probability of there not being a failure, $p + q = 1$ so that $q = 5/7$.

Now the probabilities of 0, 1, 2, 3, 4, 5 of us will suffer faulty

components are given by the terms in the series

$$(p + q)^5 = p^5 + 5p^4q + 10p^3q^2 + 10p^2q^3 + 5pq^4 + q^5$$

The particular case of three of us suffering $= 10p^3q^2$

$$= 10(2/7)^3(5/7)^2$$

$$= 5/42$$

Now arrange the shift register to cycle round 7 stages and set 2 digits so that the probability of the end lamp being alight is 2/7. Take groups of 5 readings and record how many, out of each group of five, have end lamps alight. Take as large a number of readings as you can. It is convenient to make out a sheet of paper as follows:

✓			✓		2
	✓	✓	✓		3
					0
✓	✓			✓	3
		✓		✓	2
✓		✓	✓	✓	4
			✓		1

The tick indicates that the end lamp is alight for that particular reading and the end column indicates how many times, out of 5 readings, an end lamp was alight. Since the speed of operation is high, a sufficiently high number of recordings can be made in a matter of 15–20 minutes. The higher the number of readings the greater is the chance of achieving a value close to 5/42 for the ratio: (Number of sets in which 3 occurs)/(Total Number of Sets).

Using the data you have already collected it is possible to estimate the probability that any given number of us will find faults in our cars during the first month.

After handling the shift register you will be aware of the powerful tool that is available. The following points should now be clear:

1. Binary numbers can be arranged as a set of on/off states existing in cells and indicated by lamps in the ON or OFF state.

2. These cells can accept, and transfer, their information at high speed.

3. You have the facility to multiply and divide by powers of 2 within the scope of the register.

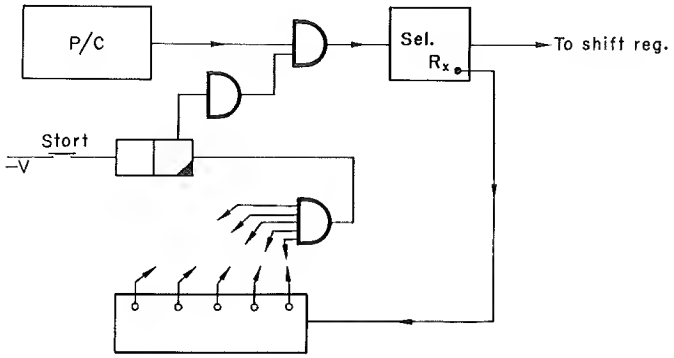
4. There is the possibility of cycling the information in a register so that it is unchanged after the operation and yet may have been used in some way during the cycling operations.

5. High speeds give you the facility of using the machine as you would a die with any number of faces up to 10 so that statistical experiments can be carried out, the machine is so fast that you cannot cheat by pressing the button at a time you feel is to your advantage unless you can judge a particular 1/50th second from all the others.

Control of the Shift Register

Our investigations so far have been on shifting operations which were either manually stopped at a desired point by restricting input to a slow rate, or were randomly stopped because the pulse rate was so fast.

We can now introduce a control system using the counter and control network. The counter can be made to count the number of shifts and then switch off the shifting pulses as soon as a desired point is reached.



This circuit shows the usual counter with control described earlier, arranged to count the number of shift operations. Since 4 pulses are needed to perform a single shift the counter must only count every 4th pulse from the clock. This is effected by counting from the R_x line which is alive for only one out of every four pulses.

Select a slow speed for the pulse clock (about $\frac{1}{2}$ sec. pulses) and set the counter to count ten, i.e. binary 01010. Enter a single digit on the register and plug in the cycle loop.

Press the start switch and observe the digit cycling round to the initial position. Reset the counter and vary the loop to cycle round 9 and notice the final position after a complete operation. Then enter cycling round 10 and vary the counter control to count 9 and observe the effect on the digit position. Next vary the counter to count 11, then 20, 21, 19, 30, 31, 29 and observe the relative positions of the initial and final digits.

Practical Exercise

Calculate the answers to the following questions and then check by setting up the problem on the shift register.

1. Enter the number 64 on the shift register and the cycle wire for 10 stages.

Which number is recorded if the counter is set for

(*a*) 6, (*b*) 7, (*c*) 17, (*d*) 27, (*e*) 23

2. Which settings, of the counter, would enable a final number of 8 to be recorded if the initial setting was 64 (i.e. binary digit entered at 2^6)—each part has more than one answer.

(*a*) if cycle wire is retained at 10?

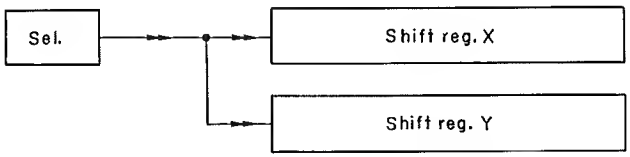
(*b*) if cycle wire is changed to 9?

(*c*) if cycle wire is changed to 5?

The speed can now be changed to high speed and all these experiments repeated to note the high speed at which these final results can be achieved. Try other binary numbers with more than one digit and observe the effect of the same operations on these numbers.

A Second Shift Register

Now construct a second shift register which can be driven simultaneously with the first from the same selector but with its own emitter follower amplifiers.



Carry out now, some of the above experiments with the second shift register in parallel with the first and observe the binary numbers cycling round together, in step.

Now let us consider some uses to which two registers can be put which do not involve addition and which are very interesting.

We have already seen that one register can be used as an electronic die so that, with two or more, we can investigate the addition and multiplication laws of probability. Consider the following example.

Example

Two football teams, say Newcastle and Chelsea, are both playing matches against other teams. If the probability of Newcastle winning is 3/5 and that of Chelsea winning is 2/7, find

(i) the probability that Newcastle AND Chelsea will both win.

(ii) the probability that Newcastle OR Chelsea will win.

1. *Calculation Method*

The probability that N AND C will win is

$$\frac{3}{5} \times \frac{2}{7} = \frac{6}{35} \text{ (Multiplication Law)}$$

The probability that N OR C will win is $1 - p$, where p is the probability that both N AND C will not win.

i.e. $p = \frac{2}{5} \times \frac{5}{7} = \frac{10}{35}$

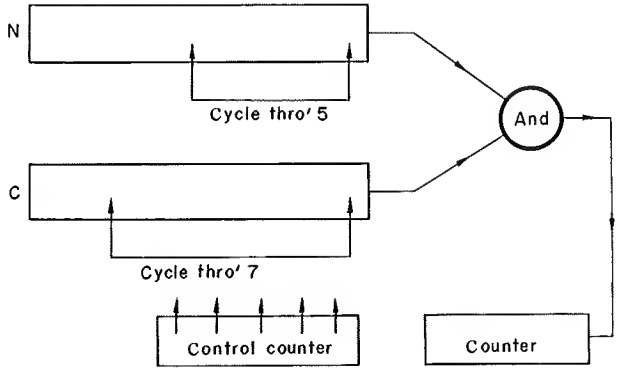
Thus probability that N OR C will win $= 1 - \frac{10}{35} = \frac{25}{35}$

$$= \frac{5}{7}$$

2. *Practical Method*

Consider the two probabilities represented on the shift registers. The first register will represent Newcastle and will be arranged to cycle through 5 stages and will have the first three stages set ON. The second register will represent Chelsea and will cycle through 7 stages and have the first two stages set ON. If these two registers are worked in parallel it will take 35, (i.e. 5×7) shifts before the two registers are in the intial state again. During this time the end two stages are both ON in 6 cases and both OFF in 10 cases. If the outputs are fed to an AND or an OR gate and thence to a counter it is possible to count the number of cases where the end two lamps

are both ON or the cases where they are not both OFF. The diagram below shows the set-up for the first case:



The control counter gives the total number of selections appearing in the end compartments while the other counter gives the number of cases where the last two compartments were ON. Provided that the control counter is set to a multiple of 35, the answer to our problem is given by the result in the counter divided by the result in the control counter. If the calculation to find 35 is not expected, then the deviation from the correct result will vary according to the reading in the control counter but will become less significent as the number in this counter reaches high values. Satisfactory completion of this problem would therefore depend on a larger counter or a set of standard counters in series.

The shift registers will not handle probability examples in which the denominators are equal or have common factors, since all combinations are not then selected.

The following exercise can be worked by calculation or by using one or two shift registers.

Exercise 4

1. The probability of a football team gaining a home win on any Saturday afternoon is estimated at 3/5. What is the probability that it will win 2, and not win the remaining match, out of 3 home matches?

2. The probability of a day being fine during the first week in August is estimated as 2/9. Find the probability that 5, and only 5,

fine days will occur during this week. Find also the probability that at least 5 fine days will occur.

3. The probability of a boy meeting, and marrying, a girl with an interest in cricket is 1/10. What is the probability that, of 6 unmarried members of a cricket club, 3, and only 3, will be lucky in choosing what, to them, will be the perfect girl?

4. The probability that a certain plant will flourish in a particular garden is 2/3. Find the probability that at least 4 out of 5 plants in the garden will flourish.

5. A candidate for an examination considers that his probability of success in mathematics is 5/7 and in physics 7/8. What is his probability of success in (i) both, (ii) only one, (iii) neither of these two subjects?

6. What is the probability that any particular person, chosen at random, is both male and was born on a Wednesday?

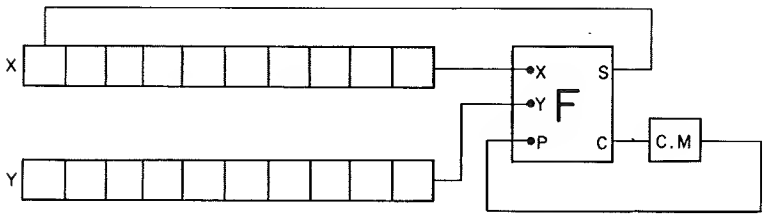
CHAPTER VII

The Model Computer

We now have the necessary building bricks for a model computer. This model should be able to add, subtract, compare, accumulate and multiply by repeated addition. These operations can be carried out at high speed or at a slow speed for demonstration of the processes or in single steps for demonstration of individual stages in the processes.

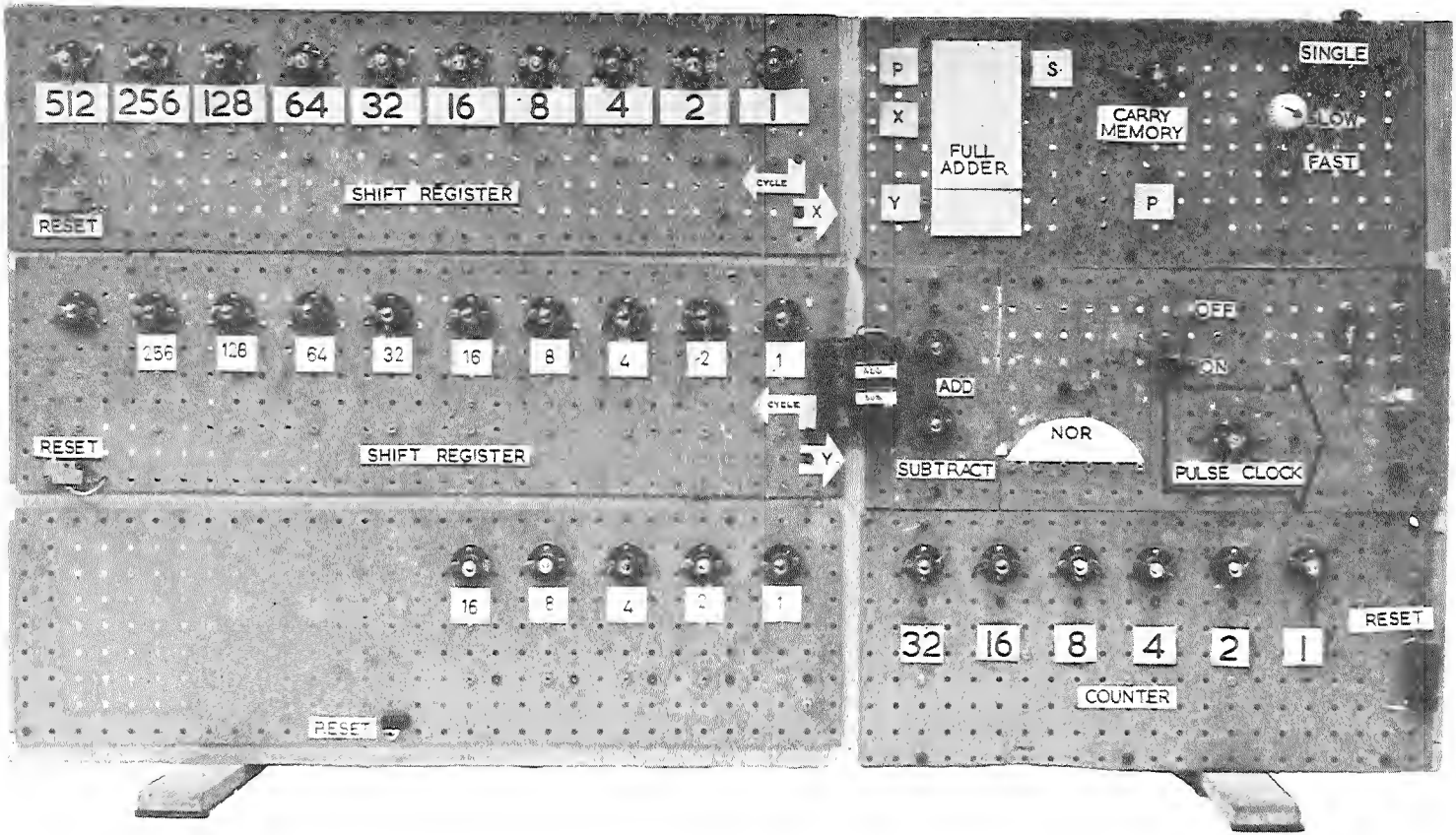
Addition

Consider two shift registers X and Y linked, as shown in the diagram below, to a full adder and a carry memory unit which is simply a single element of a shift register.



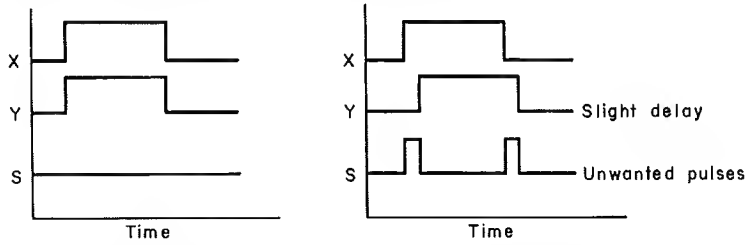
Numbers contained in X and Y are shifted to the right and enter the full adder which accepts the end digits from these registers and operates on them producing a sum result which is transferred to the end stage of the X register and a carry result which is stored in the carry memory. The second stage allows the next two digits (now at the extreme right of the register) to be fed into the full adder together with the contents of the carry memory. After 10 shift operations the sum of X and Y will be present in X, and Y will be empty unless the cycle wire had been entered.

There is however a technical difficulty here which must be overcome.

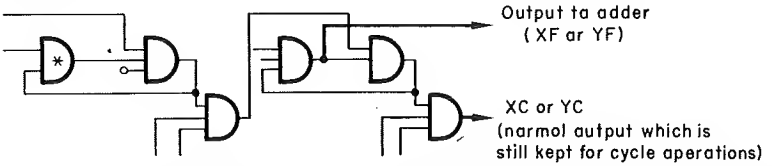


A model computer.

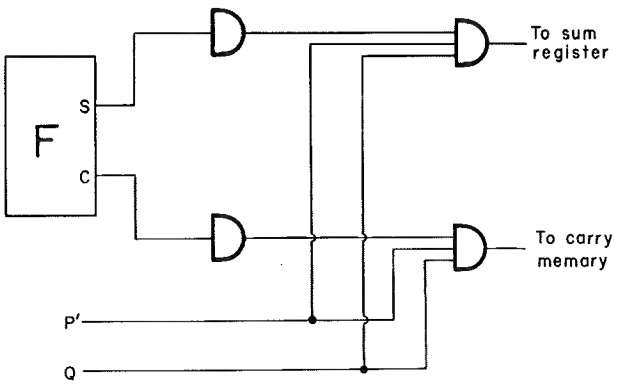
The outputs of the full adder (S and C) will set the memory cells in the X register and carry memory if they indicate '1' for a very short time—this unwanted '1' can appear if two '1' inputs to F do not arrive simultaneously so that, for a very short time, the adder acts as though 0 and 1 have been entered, and so a sum of 1 is indicated erroneously. The diagram below shows what we would like to happen and next, what may, and usually does happen.



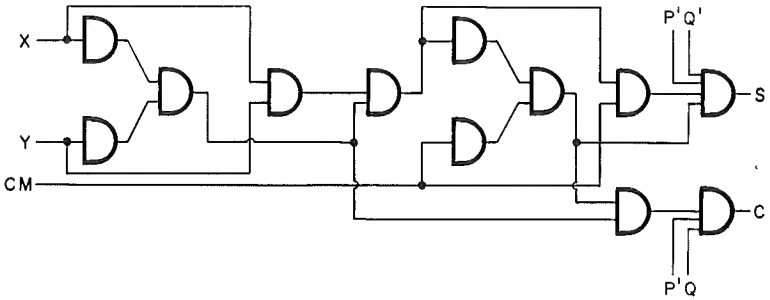
The second diagram shows the short pulses at the S output due to a delay in one of the inputs. In practice it was found that the trailing edges were together and that it was the leading edges which gave the unwanted pulse. To counteract this, the output from X, Y and CARRY is taken from a different point on the shift register element so that the full adder receives its information earlier, and for a longer time, than would be the case if it came from the normal source. This information is taken direct from the auxiliary cell, which, like the main cell, contains information for 3 pulse lengths. The following diagram shows this.



This, of course, means that the full adder would be recording outputs at S and C before it should—this is taken care of by releasing this information through a suitable gate at the normal time, thus:

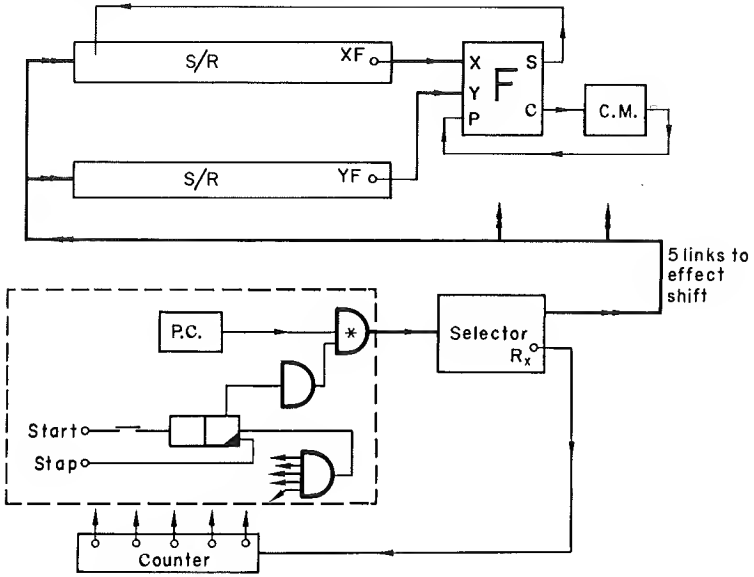


A further economy of units is possible here if the full adder is to be fully incorporated into the system. The four NOR units can be dispensed with and the release circuit, P′, Q, fed into the full adder shown completely below.



It will be seen that, not until the conditions which produce the outputs at S and C have settled down, is the information released by P′, Q. Notice that, although there are 4 inputs to the NOR unit at S, only 3 of these, at the most, are active at any one time.

The complete circuit which can now be assembled and used to add two binary numbers is given below.



These two shift registers have input sockets to each of the elements —let us call these sockets $x_1, x_2, \ldots x_{10}$, and $y_1, y_2 \ldots y_{10}$.

The special outputs to the full adder we shall call XF and YF, and the normal output, since they are used for cycle operations, XC and YC. Thus connection of XC to X_{10} allows complete cycling through 10 stages while XF to X (on full adder) feeds the contents of X register into full adder.

Operation

Check, first, that the shift registers and counters are working as described earlier, and insert links as shown.

Example

To add 11 + 1.

1. Reset counter and registers.
2. Touch x_1,x_2 and y_1 with probe. This sets 11 on register X and 1 on Y.

Set counter control to binary 1010 and use slow speed clock.

Press the start button. The two numbers are fed through the full adder and the result will appear in register X. When the counter stops automatically after 10 shifts the register X will have lost the binary No. 11 and will contain the binary number 100. The register Y will be empty unless the cycle line (YC to y_{10}) is inserted in which case the 1 in register Y will still be present. Thus we have the facility of adding two numbers and entering the result in one register and retaining one of the numbers in the other. Try sets of two numbers, first at slow speed and then at high speed. You will see that in one operation you can add two numbers, in a second operation you can add a third number to the result so that you can accumulate a result. This was not possible with the parallel binary adder without much ancillary equipment.

Now reset register and counters. Set counter to 9, cycle Y through 9 by connecting YC to y_9. Feed sum to x_9 and observe the whole operation on two binary numbers. This has the same effect as the previous operation, its only drawback being that the size of numbers chosen are limited to those with a sum involving no more than 9 digits.

We can now use one register as an accumulator and retain, or double, the contents of the other and so open the way to a sequence of operations.

Set for addition with counter on 9 stages and feed sum to x_9 but cycle Y through 10 stages. After the addition operation, register X holds the result (sum) while Y holds twice the previous contents. In this way we can sum a series such as $X + Y + 2Y + 2^2Y + 2^3Y +$ etc., and, if we take $X = 0$, we actually have a geometric series $Y + 2Y + 2^2Y + 2^3Y + \ldots\ldots$

For each addition the counter would be reset to zero unless we allowed a series of operations, in our case the limit would be three, by setting the counters to $9n$ where n is the number of operations.

Clearly we have the means here to perform simple multiplication by repeated addition and to show the usual steps in the multiplication of two binary numbers, but it would really need as much calculation to set up the computer as to perform the multiplication. This can be simplified if the counter is allowed to complete a count which is a power of 2 but to release only sufficient of these to perform the shift operations. Our model then works as follows.

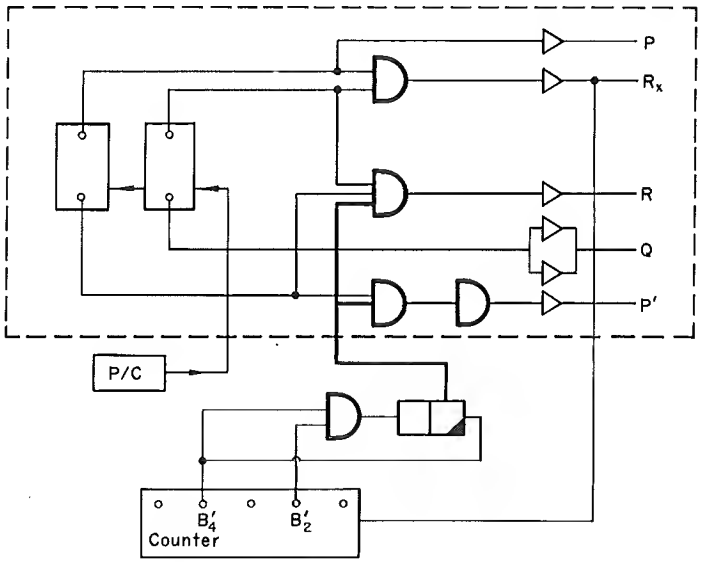
The first 10 steps will shift the registers through one complete cycle while the next 6 will be inhibited and not cause a shift. After 16 pulses the next 10 will cause shifting to take place while the next 6 will again be inhibited. This has a number of advantages:

1. By counting, automatically, every 16 shifts we can count the number of complete operations—this is not possible with 10.

2. Any demonstrations, involving a sequence of operations, clearly show each stage as there is a suitable pause, of six shift lengths, between them.

3. Future developments could use this breathing space of 6 shift lengths to feed information about the next operation to be carried out.

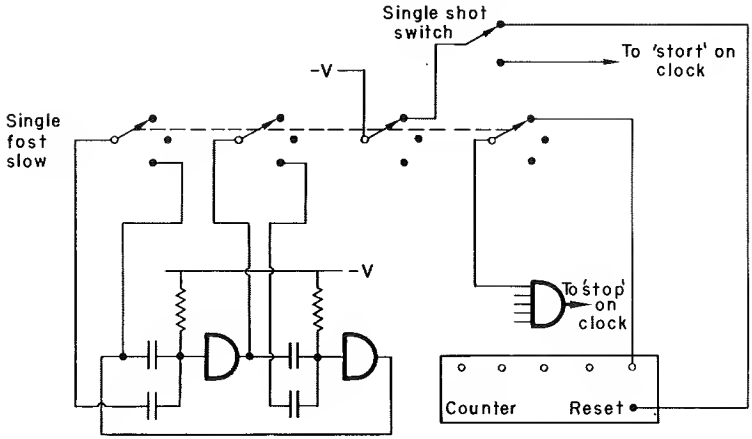
The circuit given below shows how the shift operations are inhibited for 6 out of 16 but the selector is allowed to continue to work so that the counter continues its operation. This is done by switching on a memory cell at the count of 10 and off at the count of 16. While the cell is on, it inhibits the R signals to the shift registers so that no number is cancelled and it also inhibits the flow from the



main to auxiliary cells by introducing an OR gate into the P′ circuit and so causing P′ to be live during these 6 shifts.

Speed Control

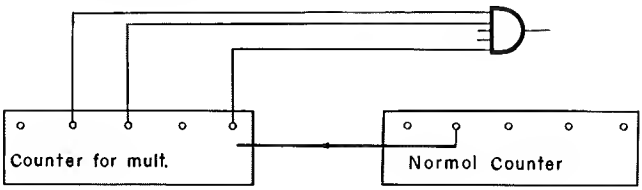
It is necessary now to be able to control the speed of these operations. The current model has a single shot switch, a slow rate of about $1\frac{1}{3}$ secs. per shift (i.e. a pulse clock rate of about 1/3 sec. per pulse) and a fast rate of 1/500 sec. per shift which gives one complete cycle time of 1/50 second. The switch over is effected by a 4 pole 3 way switch which switches in high capacitors to the pulse clock for the slow rate and leaves it out for the other two states. The single shot is really a shot of 4 pulses to effect one shift—these are produced at the high rate and the switch brings in a link from the counter B_1' to the control NOR unit. The circuit for this is as follows:



Multiplication

The procedure here, is to add the number in Y to the contents of X (zero to start with) a number of times (say Z) thus producing the product YZ in the X register.

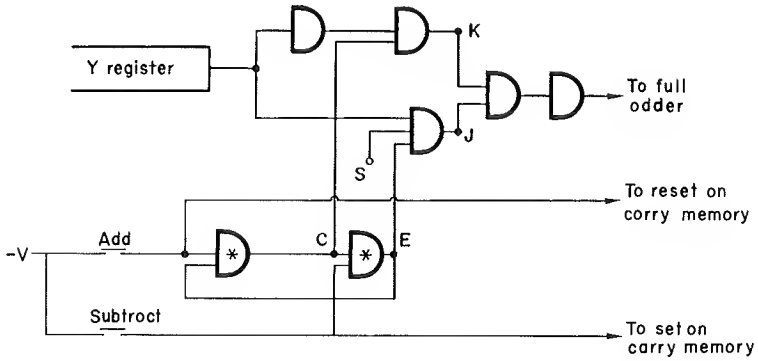
Z is selected on a second counter which is used to control the main pulse clock. The normal counter goes through the normal 10 + 6 sequence a number of times (Z) which is counted on the second clock. The circuit is shown below.



Subtraction

This is carried out by complementing the number stored in Y and adding this complement to X together with an extra '1' stored in the carry memory thus computing X — Y and placing the result in X. Although the complement is used, the number is visible in its true form so that, if 1 is indicated it is read as 0 while 0 is read as 1.

The circuit for reversing the information is basically an NOR unit but the circuit below shows a complete circuit to switch from add to subtract and vice versa.



The circuit shows 7 NOR elements, 2 of them with indicators, which will allow the true state, or the inverse state, to be supplied at the end point dependant upon which button, add or subtract, was last depressed.

The flow through the diagram works as follows:

The two indicated NOR elements form a memory cell. If the ADD button is depressed then the cell switches in such a way that the point E is live while if the SUBTRACT button is pressed then C is live. Points C and E are fed to elements which control the flow out of Y, in this way:

If YF is fed with information it could flow along the top route in the diagram to point K provided it is not inhibited by C which would be the case if the subtract button had been pressed. If C is not active, then E will be alive and flow is inhibited through the lower route from YF so that J is permanently dead. After depressing the subtract button, C becomes live and inhibits the flow through to K. While E becomes dead and allows an inverted flow through to J. K and J points are fed through 2 NOR elements forming an OR gate

so that the output is either the true or the inverse of the information stored in Y. The add and subtract buttons are also connected to the reset and set points on the carry memory—this enables the extra 1 to be entered as soon as the subtract button is pressed while the add button cancels this for any addition operations which may follow.

This complete unit can be arranged on the NOR board with a pulse flow input from a pulse clock or the manual switch. The two indicator lamps on the memory cell can be labelled ADD and SUBTRACT so that all may see the state of the network and be aware of the operation to be performed.

If the circuit on page 105 is in the subtract state, the point J will be live during the six 'rest' pulses. This can give a false result unless J is inhibited while the 6 'rest' pulses are flowing. A link from the memory cell in the 10 + 6 circuit to the point S in the add-subtract circuit will rectify this.

Comparison

You have seen how to subtract Y from X and in all our examples, $X \geqslant Y$ so that our result is positive. Notice that, after the operation has been completed, the carry memory is storing 1 ready for further subtraction if necessary. It is only necessary to press the add or subtract button when a change of operation is needed unless $X < Y$. In this instance the carry memory stores 0. You should be able to see why this is so by performing the operation in single steps:

Try (1) To carry out a simple problem on directed numbers such as $11 - 111 + 110$ where the first operation gives a result which should represent -100 and observe how this appears on the board and how the addition of a number greater than 100 restores you to the world of positive numbers.

(2) Cycle both X and Y but press subtraction button and do not feed the sum into the register. One complete cycle leaves contents of register X and Y in their original position but observe the carry memory lamp
If $X \geqslant Y$ lamp is ON
If $Y > X$ lamp is OFF

Suggestions for further development

1. A third shift register so that a result is stored in the computer without necessarily eliminating X or Y.

2. Multiplication by shifting and adding—this does need 3 shift registers and ancillary circuits, but there are no real obstacles. From the information given it should be clear how this can be performed with extra circuitry added to the model.

3. Storage—although further shift registers can be used to do this it would prove to be excessively costly. A store can be built using much less than a shift element. Economy may also be possible by restricting the size of the number to less than 10 digits.

4. Further control to enable a programme of instructions to be arranged and carried out—this is essential if the model is going to do a complete computing job. While at the moment it is capable of showing how the real computer can be built up and how the different parts function it is primarily only an arithmetic unit with simple control and storage—the input is manual and the output by means of lamp indicators. In spite of this, one can begin to see, when looking at a computer programme, just how the work will be carried out. Of course there are many operations carried out by the real computer which appear complex, but they can all be broken down into the operations we have discussed. Many of these operations may have to be performed, but they can be carried out at high speed and so produce results in a reasonable time.

CHAPTER VIII

Automatic Control

Automatic control of machines has been with us for some time—the automatic telephone exchange and the automatic lift are not new. The type of circuits which we have been discussing do, however, lend a new dimension to this control. The transistor has helped to reduce the size of the control units, has made them physically more robust and can guarantee much longer periods of trouble-free service. Lower voltages and currents save the cost of larger power units and heavy current equipment while the lack of moving parts speeds operations and avoids wear and tear.

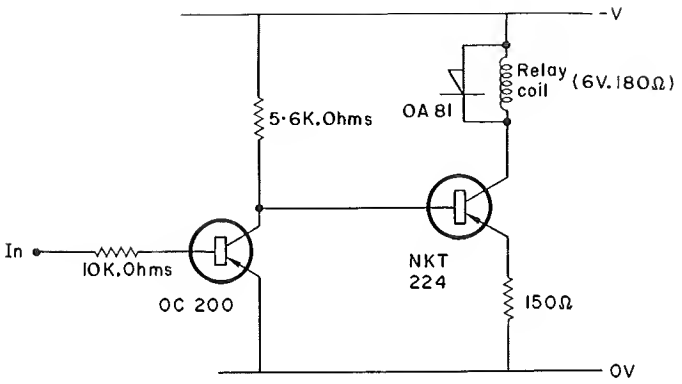
The circuits described earlier can be used to control a model railway layout but the reader will realise that many things could be controlled by these devices—the model railway appeals to schoolboys (and even more to their fathers) but the area required for a layout is large and this can present a very big problem.

The control circuits need some time to install and it is therefore desirable that any layout should be at least semi-permanent. Any layout should be very carefully assembled and every moving part checked carefully for trouble free operation before any logic control is installed.

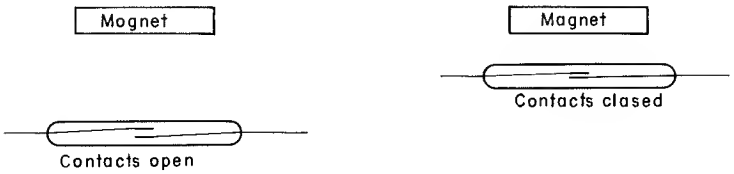
The following circuits show the basic units required to make and perform the fundamental control operations. Two devices, not previously mentioned, will be incorporated in some of our circuits, the relay and the reed switch. The relay is operated by a transistor circuit and will allow the much higher currents, needed by the layout, to be handled.

The diagram (top of page 109), shows the relay in place of the lamp.

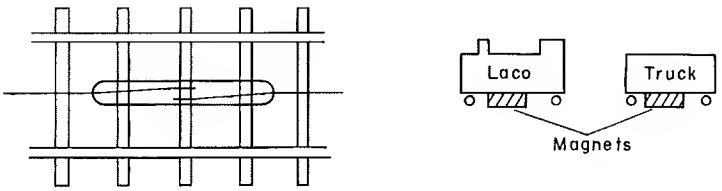
Reed switches have been introduced on to the market comparatively recently and have the advantage of being relatively cheap and small. They have contacts with a long life (being gold plated and



sealed) and they can be operated by coil or magnet without direct contact with the switch.



These reed switches, of length 0·8 inches, can be inserted between the rails of the track and the magnet fastened to the underside of the locomotive or a truck.



A '00' railway network with at least one electrically operated point and a locomotive and trucks with only 4 wheels each are recommended. The couplings should be removed so that the locomotive does not attach itself to the rolling stock and so uncoupling mechanisms need not be considered.

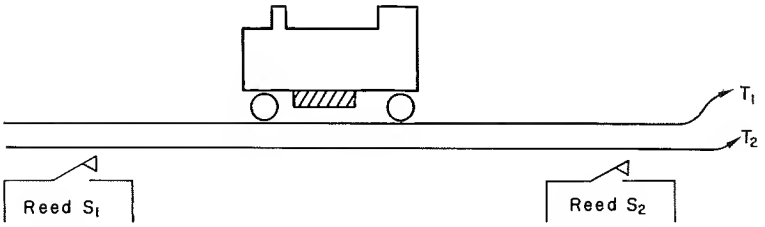
Power supplies to the track and points are supplied with the layout and should be kept separate from those of the logic circuits to be used for control.

Demonstration No. 1

Continuous motion of a locomotive between two points on a linear track:

Apparatus

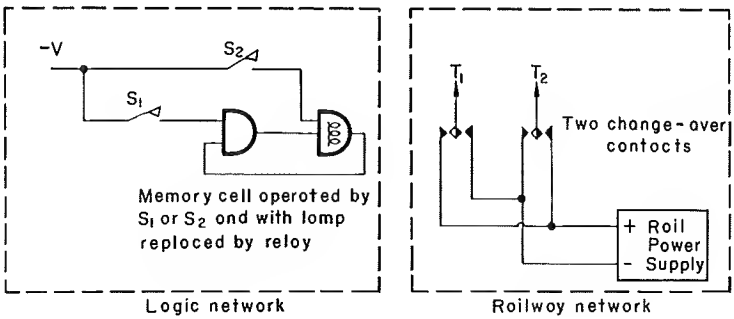
One length of track at least 3 feet long
One locomotive with small permanent magnet attached
Power supply for railway layout
1 NOR unit with relay circuit containing two change-over contacts
1 normal NOR unit
2 Reed switches



The diagram above shows a length of track with a supply applied to rails T_1, and T_2 of the track. Reed switches S_1 and S_2 are inserted about 6 in.—9 in. from the two ends of the track and are normally open. The locomotive with a magnet attached passes over and operates the switch. The magnet should pass as close as possible and be parallel to the switch but should not be lower than the top of the rail otherwise it would not pass freely over a set of points.

We will now arrange a circuit to allow the locomotive to travel backward and forward between S_1 and S_2.

The two rails on which the loco runs we shall call T_1 and T_2. These rails are + and − for a journey from S_1 to S_2 and reverse their polarity for the journey from S_2 to S_1. The changeover is effected by means of a relay which is part of a memory circuit. Closing of S_1 activates the relay coil, sets T_1 positive and T_2 negative while closing of S_2 sets T_1 negative and T_2 positive as is shown in the following diagram.

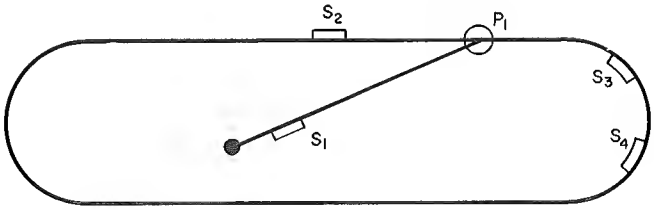


Demonstration No. 2

To cause a locomotive to deposit a truck, when available, in a siding and then continue to circulate.

Apparatus

As for the last demonstration plus:
Trucks (any number) with magnets attached
1 electrically operated point
2 additional reed switches
2 delay circuits arranged to operate relays with make/break contacts
1 memory cell



Form a closed loop, with one siding. Insert 4 reed switches S_1,S_2, S_3,S_4 in the positions indicated. P_1 is a point which can be set straight ahead or left. In the straight ahead position the loop is closed and a loco on this loop could run indefinitely. In the left position the loco whose forward run was in the anti-clockwise direction would enter the siding. The points on a model train layout are changed by means of one of two coils. One coil, when activated will pull the points to the left the other to the straight ahead position. The current flow through these coils, is relatively high and should not be allowed to flow for long (say 1 to 2 seconds) otherwise these coils will burn out. This adds certain difficulties to our circuit for we must arrange that the flow of current is terminated after approximately 1 second. Now let us see what we want to do with this circuit.

With one locomotive on the track the loop will be closed and the locomotive will travel in the anti-clockwise direction. If a truck is placed anywhere on the loop the loco will push this round until it reaches P where it will be diverted into the siding. Before it reaches the end of the line the direction of motion will be reversed and the truck will be deposited and the loco return to the loop. Once firmly established in the loop the direction of motion will again change and the points will change so that the loco travels in the loop until a new condition is applied to the circuit.

Let us reduce this problem to a set of logical statements:

1. If a loco and no truck, then P is straight ahead and the direction of the loco is straight ahead. This may, or may not, be the state of the whole circuit when we place the loco on the track. If it is, all is straightforward, but if it is not then a change must take place.

Switch S_2 takes care of this and should be as close as practicable to P on the side indicated. The loco is placed on the track and will proceed either forward or backward. If forward this is straightforward, if backward it will activate S_2 which will change the state of points P_1 to ahead and change the direction of motion of loco ahead. This circuit is identical to the one in the previous layout.

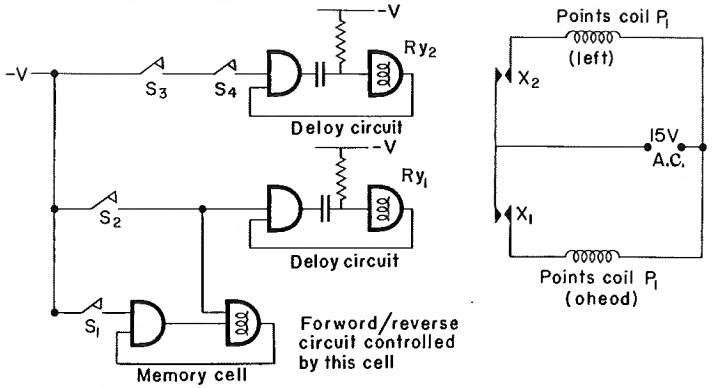
2. If a truck is added then P changes to left so that train will enter siding. This is effected by S_4 and S_3 being closed simultaneously.

3. If a train enters siding the direction of motion must be changed so that it does not reach end of line. This is effected by S_1.

In short if S_2 then *forward* and points *ahead*

if S_1 then *reverse*

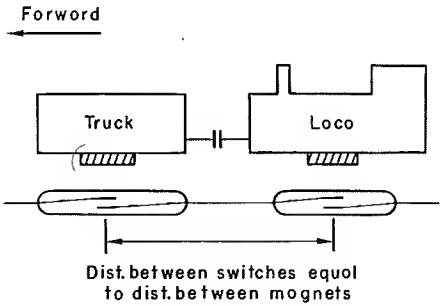
if S_3 *and* S_4 then points *left*



X_2 normally open contacts on relay Ry_2

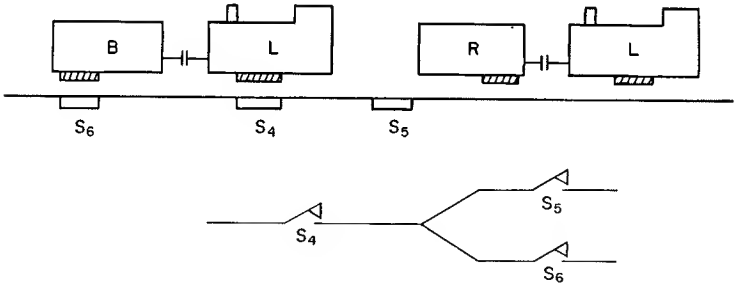
X_1 normally open contacts on relay Ry_1

The simultaneous operation of S_3 and S_4 is best explained by the following diagram



From the last circuit you will see how to operate forward-reverse and point mechanism.

As more equipment such as points, switches and logic circuits, become available then bigger and more complex operations can be carried out. The idea given in this chapter should be sufficient to enable a lot more to be done—above all, if you can change direction and points then much can be done.



Slight displacements of magnets to the front or rear of a truck can enable different trucks to be recognised.

Thus R and L operate S_5 and S_4 simultaneously.

B and L operate S_6 and S_4 simultaneously.

Arrangements like this would enable trucks to be sorted—say red trucks into one siding and blue into another.

Remember that any circuit which is supposed to think out a course of action must be very carefully designed so that all possibilities have been considered. For example, in our layout, it is possible to start with the state of the points either left or ahead and the direction clockwise or anti-clockwise and the system will work. The satisfactory working does, however, depend on the momentum of a truck carrying it over S_1 during the depositing operation so that the reverse circuit is not held on.

Try to design a few circuits—even if a layout is not available the exercise can be most enjoyable. Developments to more involved circuits will follow quickly once the simple stages outlined already have become familiar. Remember that the binary counter can be used to count trucks, and other devices, such as photo-electric cells, can add new dimensions to the activity.

CHAPTER IX

Power Supplies

In all the circuits described in the book zero volts and −v (negative) have been indicated. The requirements of the power supplies for these circuits are thus: earth on the positive side and a negative supply voltage of something between 12 and 15v. Although the actual value of the voltage from the power supply is not too critical, because of current changes as the circuits are switched on and off, the demands on the power supply become severe. Imagine a state in which ten logic elements, each with indicators, are all switched together. Since each bulb takes 40 mA then a total current change in the system of approximately 400 mA, nearly half an amp will have occurred. The perfect power supply is one which would give out a constant voltage irrespective of the power drawn from it. However, no power supply is perfect and a discussion of the types of power supply used may prove helpful.

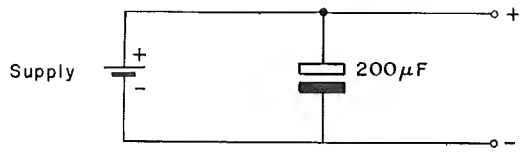
1. *12 v Car Battery*

This source has been found reasonable for most of the circuits described since it is capable of delivering quite large currents, this implies that the car battery has a very low internal resistance. Since the currents consumed by the transistor circuits are small compared to the current capacity of the car battery no appreciable voltage drop ever occurs. This is a relatively cheap source of power and is readily available. Its main disadvantages are its weight and need for regular recharging. In constant use its life expectancy can be no more than two or three years.

2. *Dry Batteries*

To our knowledge there is no dry battery of suitable capacity currently available, however, for a few logic circuits with only one or two indicator lamps, a dry battery of the type which is found in the larger transistor portable radio sets will suffice for a short time providing that counting circuits are not to be used. It may also

suffice to drive counters providing that a large capacitor is connected across the terminals of the battery, as shown in the diagram.



This is a comparatively easily attainable source of power but a very expensive one.

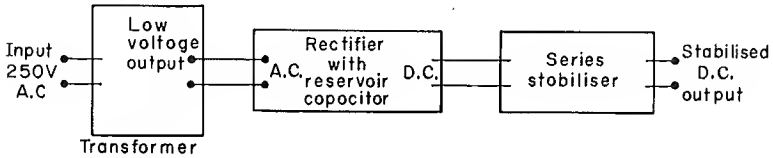
3. *Rectified A.C. Supply*

A number of circuits exist to produce rectified A.C., using half wave, full wave, or bridge rectification. A full wave, or bridge rectified, circuit is quite suitable to drive small circuits provided a large reservoir capacitor is connected across the output terminals. The only problems which occur are

(i) the output voltage is dependent slightly on the load current taken;
(ii) the residual A.C. ripple may become large enough to switch spuriously bistable circuits when high currents are being drawn from a power supply if the reservoir capacitor is not sufficiently large.

4. *Rectified and Stabilised Supply*

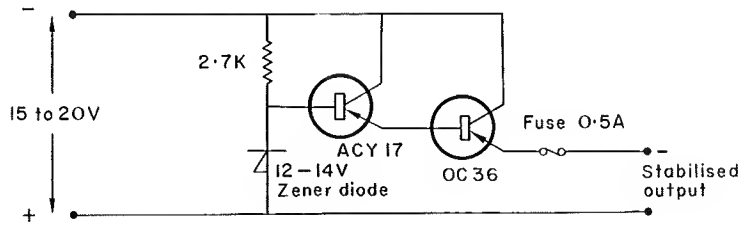
To supply the larger currents needed by models of the size of the computer a power supply with very low output impedance i.e. well stabilised power supply supplying a very constant output voltage, is needed. The way this is achieved is shown in the block layout below.



An input voltage to the stabiliser of some 5 to 10 v greater than the required output voltage will result in a quite smooth and constant output voltage, typical resistances of this type of power supply fall to 0·001 ohm. Series stabilisers may be readily purchased at a cost not much greater than any unit which could be built, therefore it is suggested that one of the commercial stabilisers be bought. Care should be taken to observe the following points:

(i) The current reading of the transformer should be sufficient to cope with the current required for the circuits.
(ii) A stabiliser should be chosen with a sufficiently high output current to cope with both present requirements and any extensions envisaged.

For any who may wish to construct a simple stabiliser a suitable circuit would be as shown.



The Zener diode connected to the base of TR1 keeps this point at constant voltage, irrespective of output currents. Since, when a transistor is conducting, there is always about 0·5 v across the base emitter diode the output voltage is always constant at a voltage approximately 1 v less than the voltage of the Zener diode. As the output current changes so would the voltage from the bridge rectifier unit. This is compensated for by a similar change in the opposite direction of the collector emitter voltage of TR2. The stability of the power supply therefore is dependent slightly on the characteristics of both the transistors and of the Zener diode. It is possible, and is generally practised, in commercial stabilisers not only to build a series stabiliser but also to provide further feedback to correct any small variations of output voltage which may occur. This is done using a rather different circuit to the one shown. Commercial units also generally include some form of current limiting device so that, if an excessive current is demanded of the series stabiliser, the voltage output from the stabiliser falls nearly to zero. This extra production has an advantage in that it both protects transistors of the stabiliser, and the circuits which the stabiliser is supplying. It must be appreciated that even if a fuse is included somewhere in the power supply line this may not act sufficiently quickly, i.e. the fuse wire may not burn out sufficiently quickly, to prevent damage to the transistors in a stabiliser or in the logic circuits. The use of heat sinks, particularly for the OC36, are recommended so that the unit does not suffer from overheating.

It would appear that the most effective way to supply power to anything but a small temporary transistor circuit would be by the last method. If power units are to be constructed it should be remembered that thorough testing by a skilled engineer should be insisted upon for any unit using the mains supply. Most educational establishments have small, portable low-voltage D.C. supplies and it is suggested that these be used, a series stabiliser be purchased, and therefore at no stage could the possibility of serious electric shock arise.

Answers to Exercises

CHAPTER II

Exercise 1

1. Output: 1,0,0,0.
   Function: A′.B′.

2. Q: X′; T: X; Q column 1,0; T column 0,1.

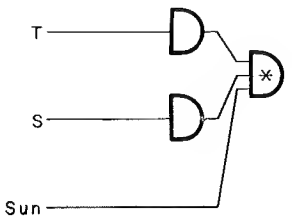
3. Function X′. Simpler circuit: only one NOR unit.

4. (i) 0; (ii) 1; (iii) X.Y′.

CHAPTER III

Exercise 2

1.



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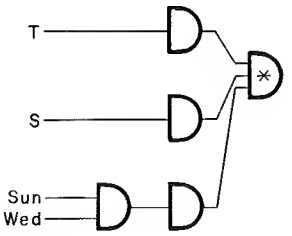

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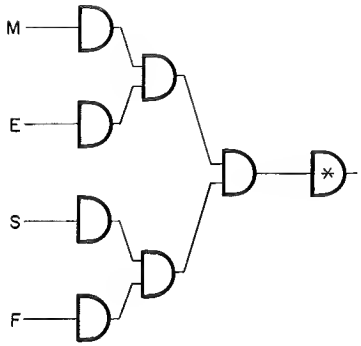

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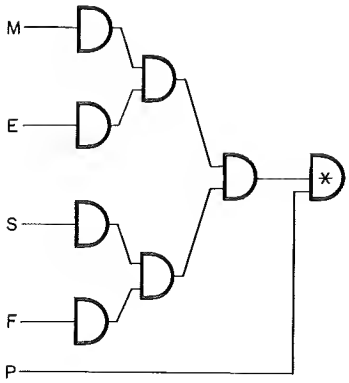

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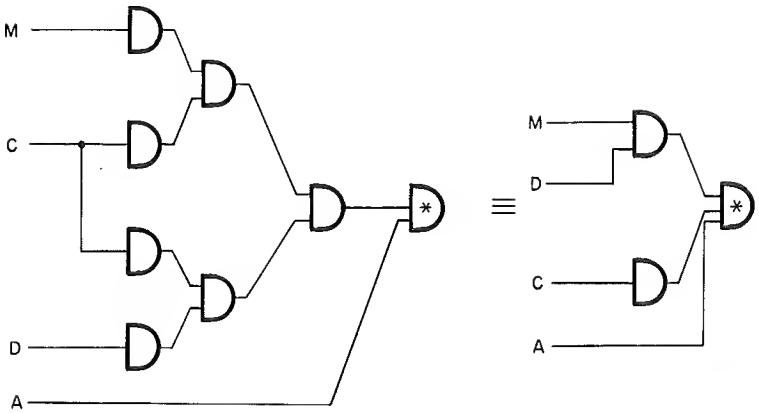
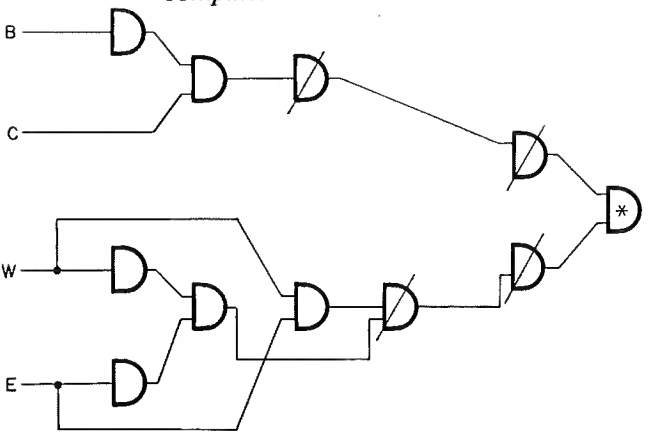


6.



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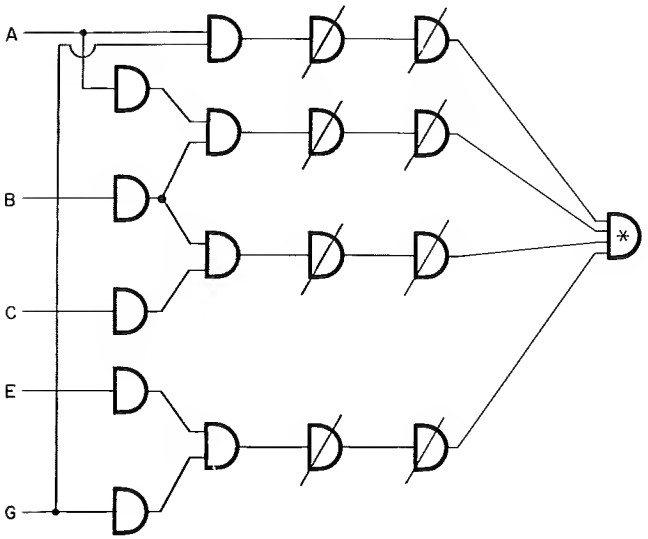

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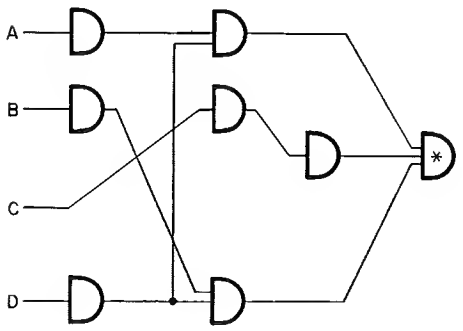

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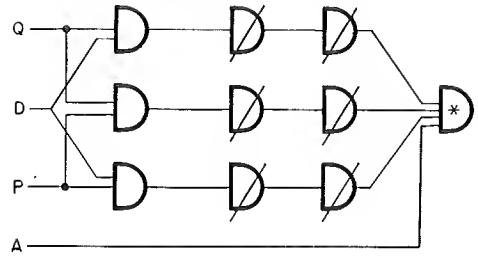
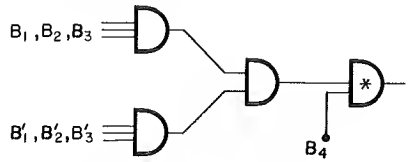


CHAPTER V

Exercise 3

1. 8 NOR units connected to the first three stages of a counter as follows:
   NOR unit representing 0 to $B_1\ B_2\ B_3$
   1 to $B_1'\ B_2\ B_3$ 2 to $B_1\ B_2'\ B_3$
   3 to $B_1'\ B_2'\ B_3$ 4 to $B_1\ B_2\ B_3'$
   5 to $B_1'\ B_2\ B_3'$ 6 to $B_1\ B_2'\ B_3'$
   7 to $B_1'\ B_2'\ B_3'$

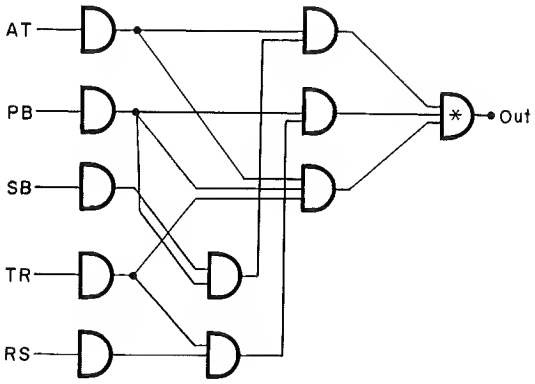
2. Red: Output of OR gate fed by B_1, B_2, B_3 and inhibited by B_4
   Amber:



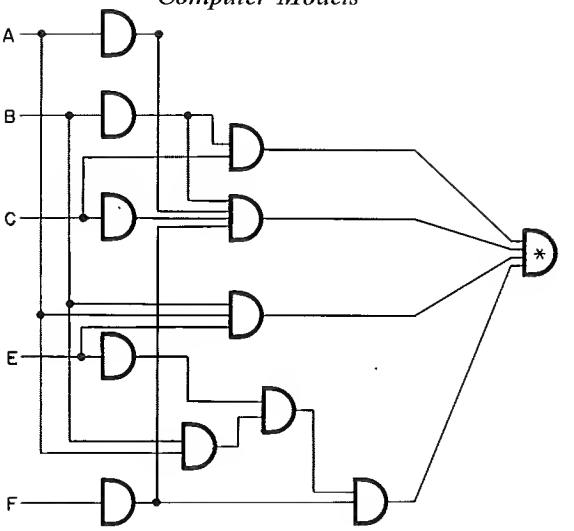
   Green: Output of a NOR unit fed by B_4'

3. (i) Output of NOR fed by B_5'
   (ii) Output of NOR fed by B_3,B_4,B_5.
   (iii) Output of memory cell in which the STOP is controlled by the output of a NOR fed by B_1', B_3' and the START by the output of a NOR fed by B_3, B_4, B_5.

4.



5.



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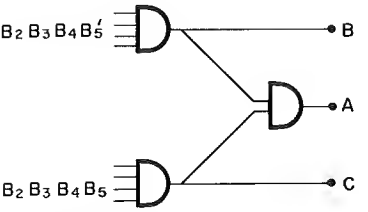


7. M_1 output of NOR fed by $B_1' B_2$
   M_2 output of NOR fed by $B_1 B_2'$
   M_3 output of NOR fed by $B_1' B_2'$
   Memory cell of pulse clock switched off by signal From B_3.

CHAPTER VI

Exercise 4

1. $\frac{54}{125}$

2. $\frac{32928}{4782969}$ = approx. $\frac{7}{1000}$ $\qquad$ $\frac{55008}{4782969}$ = approx. $\frac{1}{100}$

3. $\frac{1458}{1000{,}000}$ = a little better than 1 in 1000

4. $\frac{80}{243}$

5. (i) 35/72 (ii) 35/72 (iii) 2/72

6. 1/14

Appendix

Details of Components

The components used in the construction of the models described are all readily available on the open market. Since they are not surplus items there should be no difficulty in finding replacement parts or in extending any part of the system. There is no objection to using cheaper materials or parts removed from old electronic equipment but it is suggested that the basic units should use the recommended transistors or their direct equivalents. These have been found to be highly satisfactory and a great deal of investigation was undertaken before they were selected. Cost was considered and no excessively costly device has been chosen.

The monthly electronic and radio magazines have many advertisements listing bargain offers of components and many advertisers will quote reasonable prices for the components you need. Main manufacturers of components will either supply direct or will give the name and address of a local supplier.

The following list will give some indication of what to look for when purchasing materials:

Transistors

It is suggested that the Mullard OC200 or the Texas Instruments 2N3702 be used in the NOR circuit and the Newmarket NKT224 or the Mullard OC72 be used as the lamp transistor. If any other transistor is tried in the NOR circuit it must be a PNP silicon device and that unit should be tested under its worst load conditions before it is regarded as satisfactory. It should be remembered that a NOR unit must be capable of functioning at high speeds with possibly a varying number of inputs and outputs. There is no doubt that a small reliable system is very much better than a large unreliable system. The price of silicon transistors has fallen considerably over the last two years and there is therefore considerable saving if large quantities are purchased. Suitable transistors are available for between 1/6d and 3/-.

Diodes

The OA81 is a good general purpose diode and no alternative is recommended.

Capacitors

These are not critical and old capacitors removed from scrap equipment have often been found to be satisfactory. It is pointed out,

however, that most of the capacitors are 0·01uF and are very cheap. The capacitors used in the logic circuits are rated at 15 volts and in the smoothing circuits at 25 volts. These are both minimum voltage ratings.

Resistors

All resistors used in the logic circuits are ½ watt types that can be found in some old electronic equipment and these may be perfectly useable. Since, however, many of the resistors used are either 10k. or 5·6 k. ohms, advantage can be taken of the cheaper rates when buying these in bulk, when they can be purchased for a little more than a penny each.

Miniature Sockets and Plugs

This is the name given to a type of socket and plug which fits the holes in standard peg-board and which is ideal for the job from every point of view including cost.

Relays

For use in conjunction with the logic system, a relay should operate satisfactorily at 6 volts, and have a minimum coil resistance of 180 ohms. A dust cover to protect the relay contacts would be helpful.

Reed Switches

Since these are not required to carry high currents the smallest size component, consistent with low cost should be used.

Lamps

The recommended lamp is rated at 6 volts, 0·04 amps and it is unwise to change this.

Voltage Stabilisers

A stabiliser will supply a given output voltage at up to a stated current. The higher the stated current, the higher the price of the stabiliser. It is suggested that 3 amps is a reasonable value for this current and such a unit is less than twice the cost of the 1 amp model. The voltage input to the stabiliser must be about 5 volts higher than the output even when under full load.

Test Equipment

Any multimeter with a sensitivity of 20,000 ohms per volt is very satisfactory provided it has a range which will measure from 1 to 20 volts and one which will measure resistance of the order of 10 k. ohms.

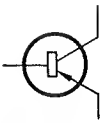
List of Manufacturers and Suppliers

Texas Instruments Ltd., Supplies Division, 12 Wellcroft Road, Slough, Bucks; Newmarket Transistors Ltd., Exning Road, Newmarket, Suffolk; A. C. Farnell Ltd., Hereford House, North Court, Vicar Lane, Leeds 2; Radiospares Ltd., 4–8 Maple Street, London, W.1; Radio & Television Services Ltd., P.O. Box 11, Gloucester Street, Cambridge.

Bibliography

Abrahams & Thomas	*The Lan-Dec Digital Educational Computer Handbook*	Lan-Electronics
Adler	*Thinking Machines*	Dobson
Bolt	*We Built our own Computers*	C.U.P.
Budden	*An Introduction to Number Scales and Computers*	Longmans
Flanagan & Molyneux	*A Slow Speed Single Supply NOR Logic System*	Electronic Engineering July 1964
	A System of Logic for use in Teaching Mathematics	A.T.M. Magazine No. 30 Spring 1965
Flegg	*Boolean Algebra and its Application*	Blackie
Glicksman & Ruderman	*Fundamentals for Advanced Mathematics*	Holt, Rinehart & Winston
Hersee	*A Simple Approach to Electronic Computers*	Blackie
Lovis	*Computers I and II*	Arnold
	Contemporary School Mathematics Series	Arnold
Marchant & Pegg	*Digital Computers— A Practical Approach*	Blackie
Murphy	*Basics of Digital Computers*	Rider
Whitesitt	*Boolean Algebra and its Applications*	Addison Wesley
Wilkinson	*A Small Computer Model*	A.T.M. Magazine No. 32 Autumn 1965
	A Computer Logic Demonstration Board	A.T.M. Magazine No. 32 Autumn 1965

List of Symbols Used

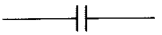


Transistor

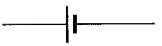
Base view of transistor Type OC200

Base view of transistor Type NKT224

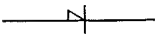
Resistor



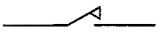
Capacitor



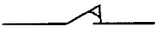
Low voltage cell



Diode



Switch (normally open)



Switch (normally closed)

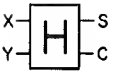
Push (to make) switch

NOR unit

Index

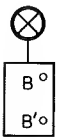
NOR unit with lamp indicator

Lamp

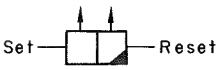


Half Adder

Full Adder



Scale-of-Two Unit with lamp remote from unit and points B, B′ which are respectively live and dead when the lamp is ON.



Memory cell in which the righ-hand cell is live after pulse applied to set point, and left-hand cell is live after pulse applied to the reset point.

Symbols Commonly Used in other Publications

Two symbols for NOR unit

'OR' Gate, any 1 live input causes a live output.

'AND' Gate, 3 live inputs cause live output.

SBN: 7131 1505 X